SHARP

T03i5VL-E30//

1993

LIQUID CRYSTAL CAMCORDER 8
TECHNICAL MANUAL

MODELS VL-E30S/H/X/E7E/D
VL-E30U/C/E35U/E35
VL-E40S/H/X/E8E/D
VL-E40U/C

CONTENTS

SHARP CORPORATION

MECHANICAL SECTION

1. DESCRIPTION OF MAJOR PARTS IN THE MECHANISM AND PARTS LAYOUT VIEWS

1-1. Automatic Discrimination Mechanism for the 8 mm Video Cassette

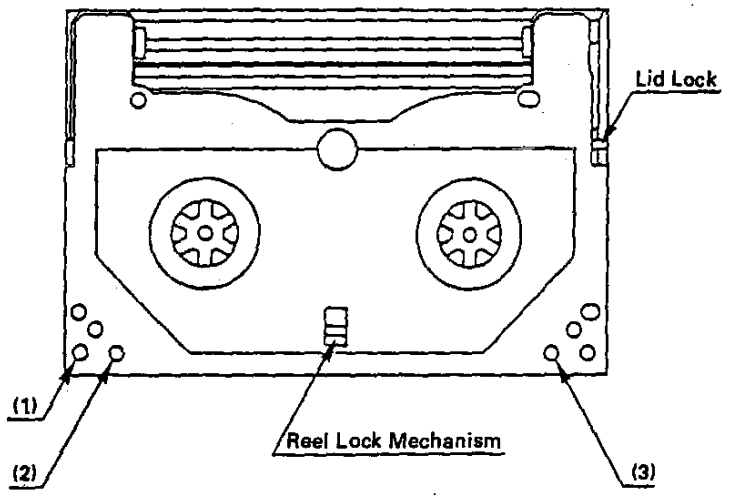
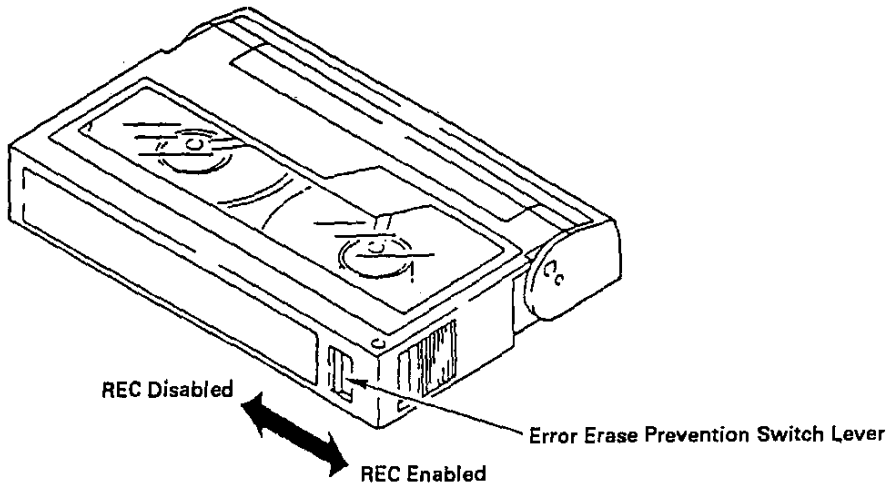


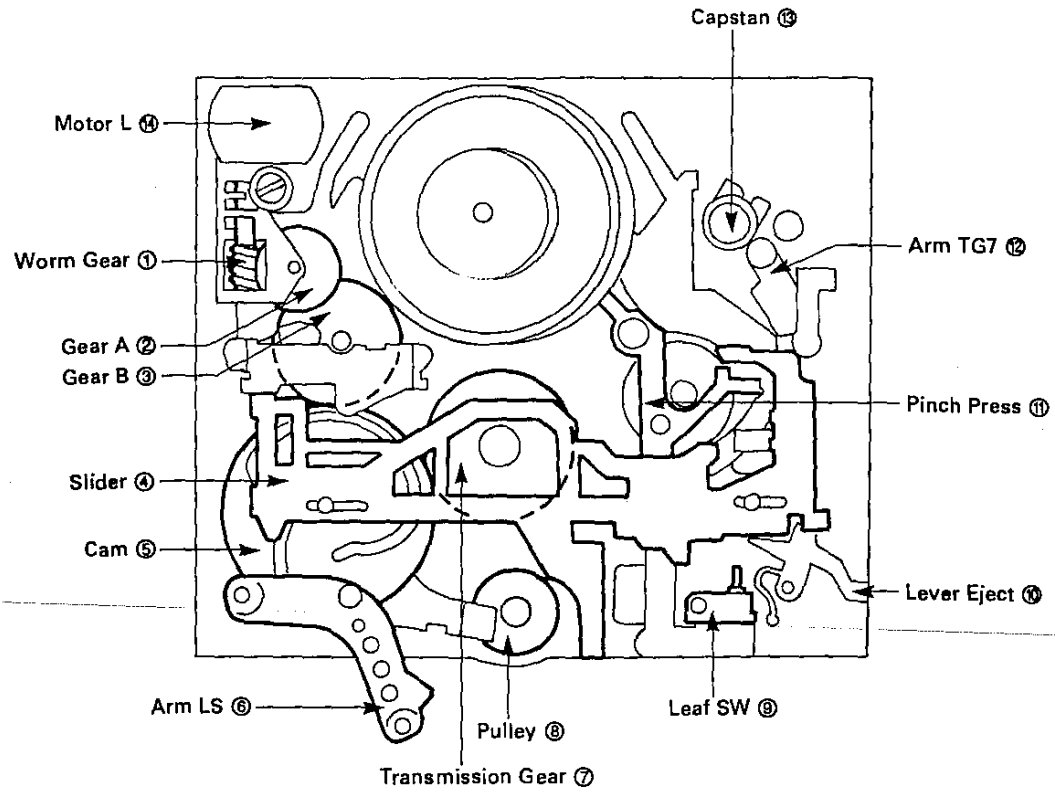
Table 1

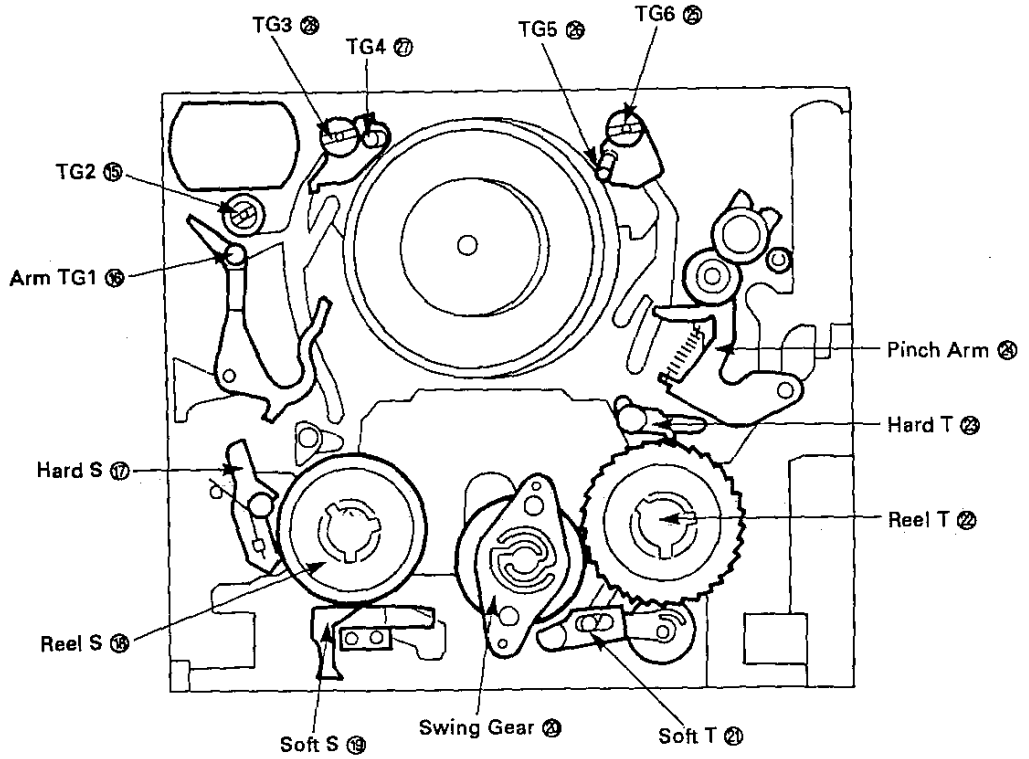
	Object	Closed	Opened
(1)	Error Erase Prevention Switch Hole	REC Enabled	REC Disabled
(2)	Tape Type	Type A (MP Tape)	Type B (ME Tape)
(3)	Tape Thickness	13 μm Tape	10 μm Tape

Fig. 1 View of Cassette Bottom



1-2. Positions and Names of Major Parts in the Mechanism

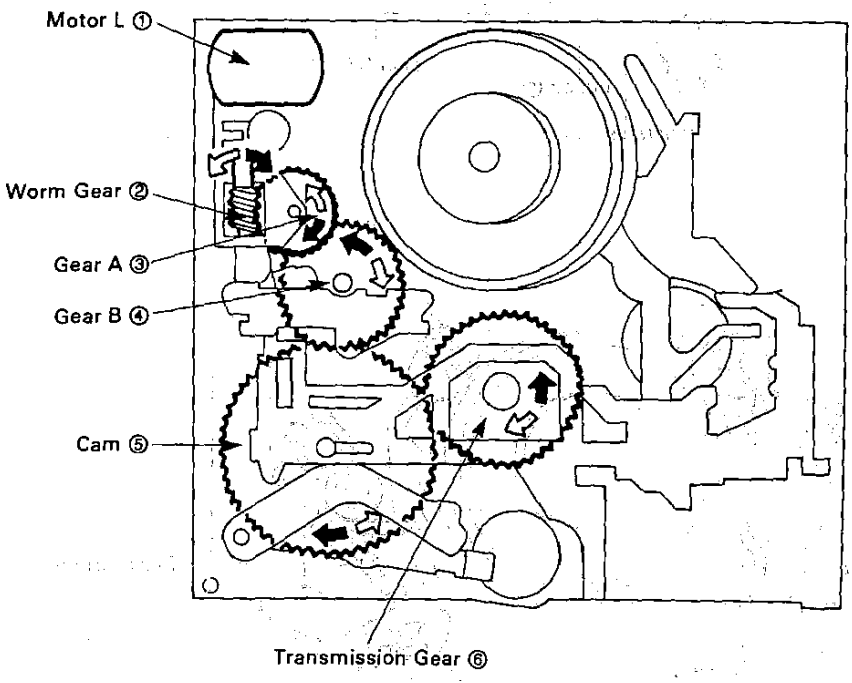




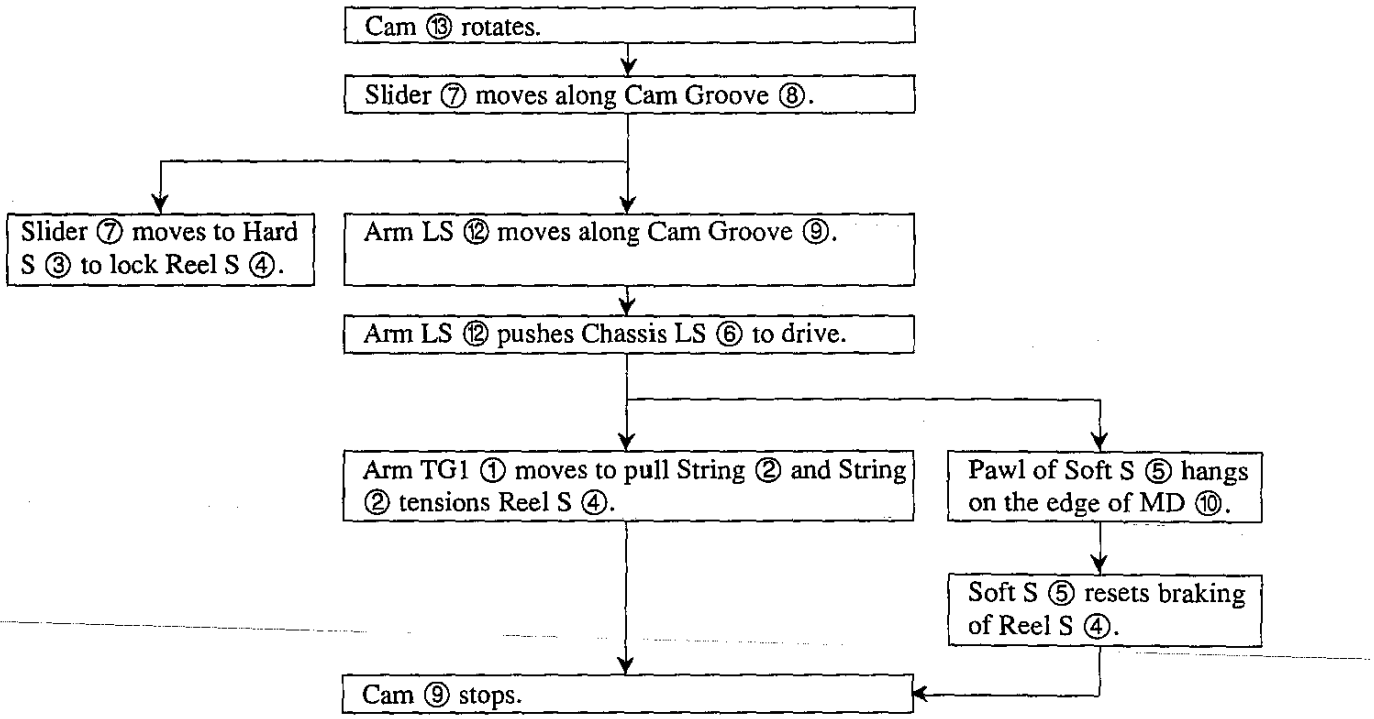
2. DESCRIPTION OF STRUCTURE IN EACH UNIT

2-1. Gear Train

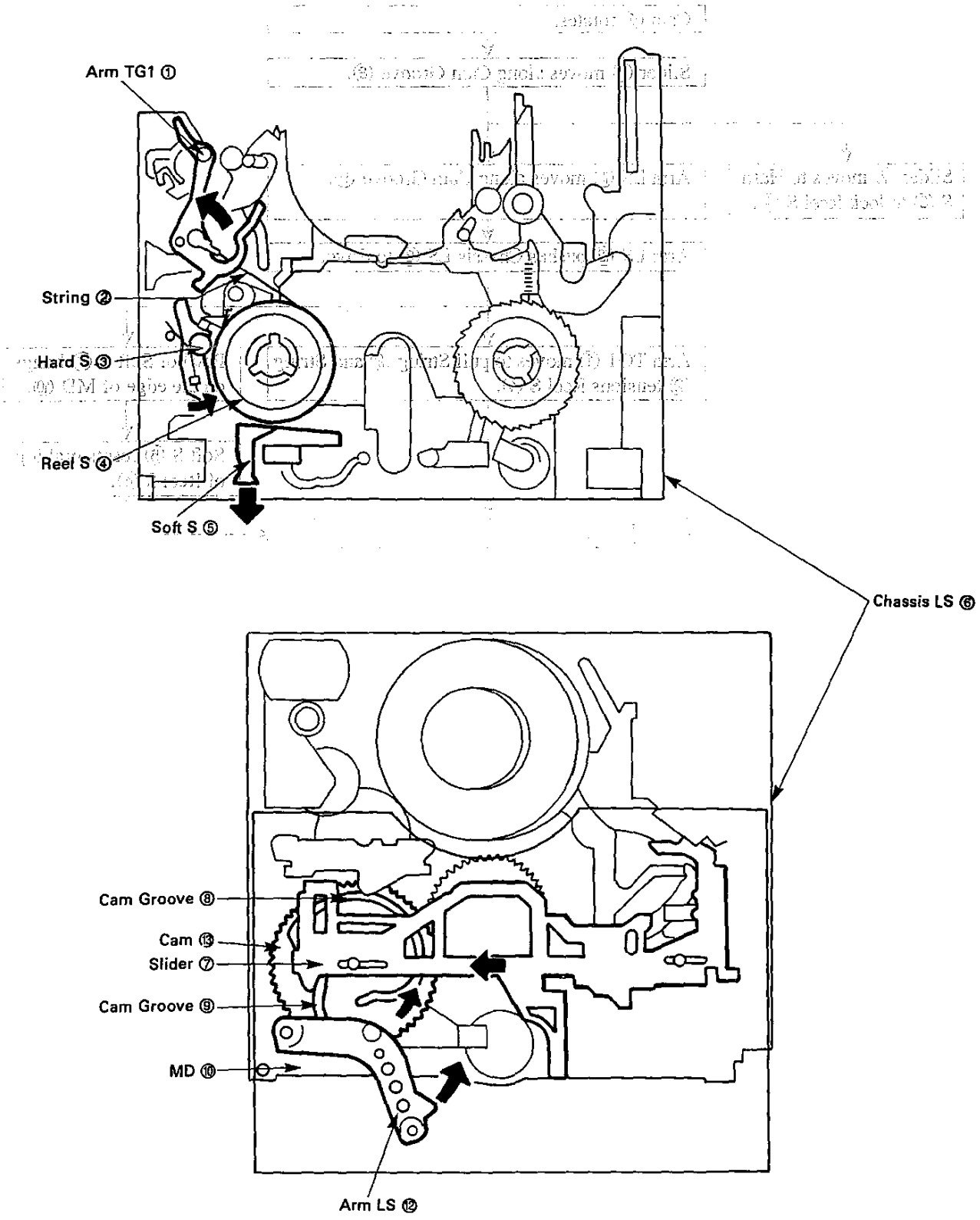
Motor L ① rotates.
↓
RPM is decreased by Worm Gear. ②
↓
RPM is further decreased by GearA ③.
↓
Gear B ④ rotates.
↓
Cam ⑤ rotates.
↓
Transmission Gear ⑥ rotates.



2-2. Brakes S Soft and S Hard

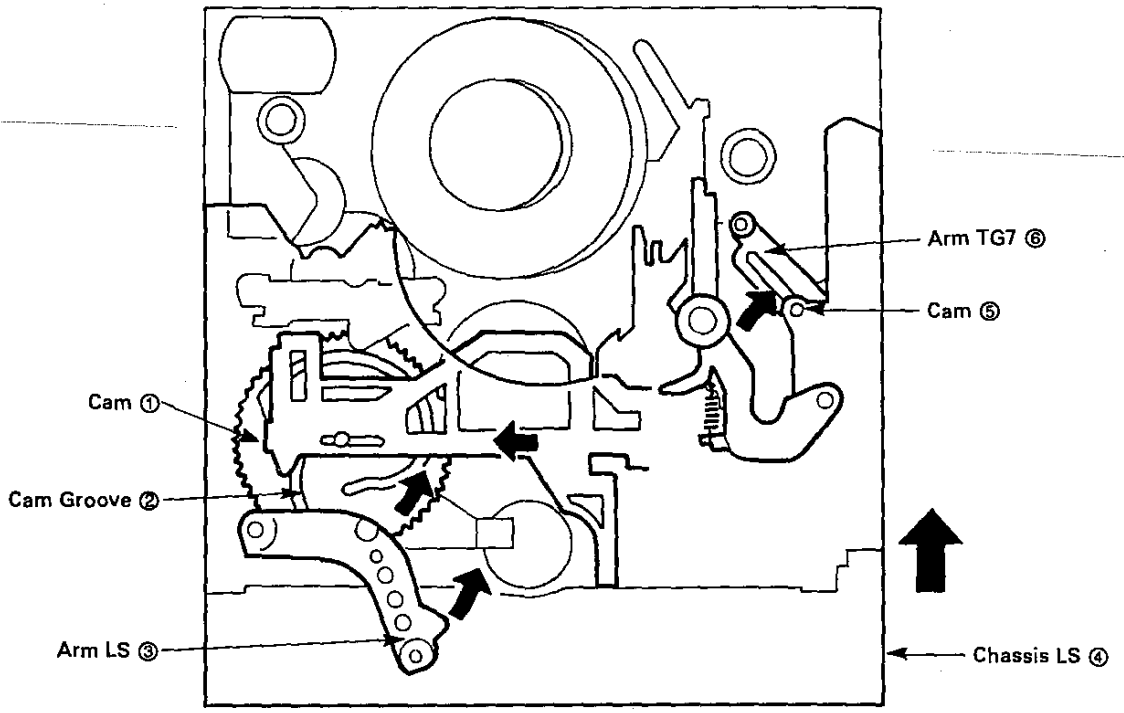


Brake S


Arm TG1 ①
String ②
Hard S ③
Reel S ④
Soft S ⑤
Chassis LS ⑥
Cam Groove ⑧
Cam ⑬
Slider ⑦
Cam Groove ⑨
MD ⑩
Arm LS ⑫

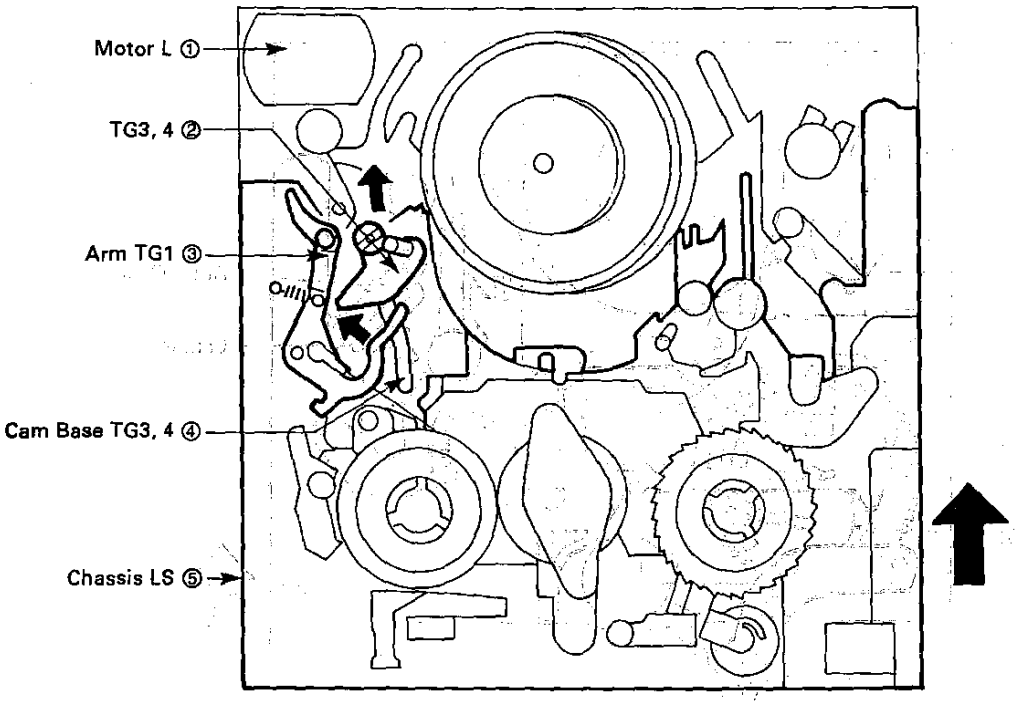
2-3. Chassis LS and Arm TG7

Cam ① rotates.
↓
Arm LS ③ moves along Cam Groove ②.
↓
Chassis LS ④ slides.
↓
Arm TG7 ⑥ moves along Cam ⑤ of Chassis LS ④.



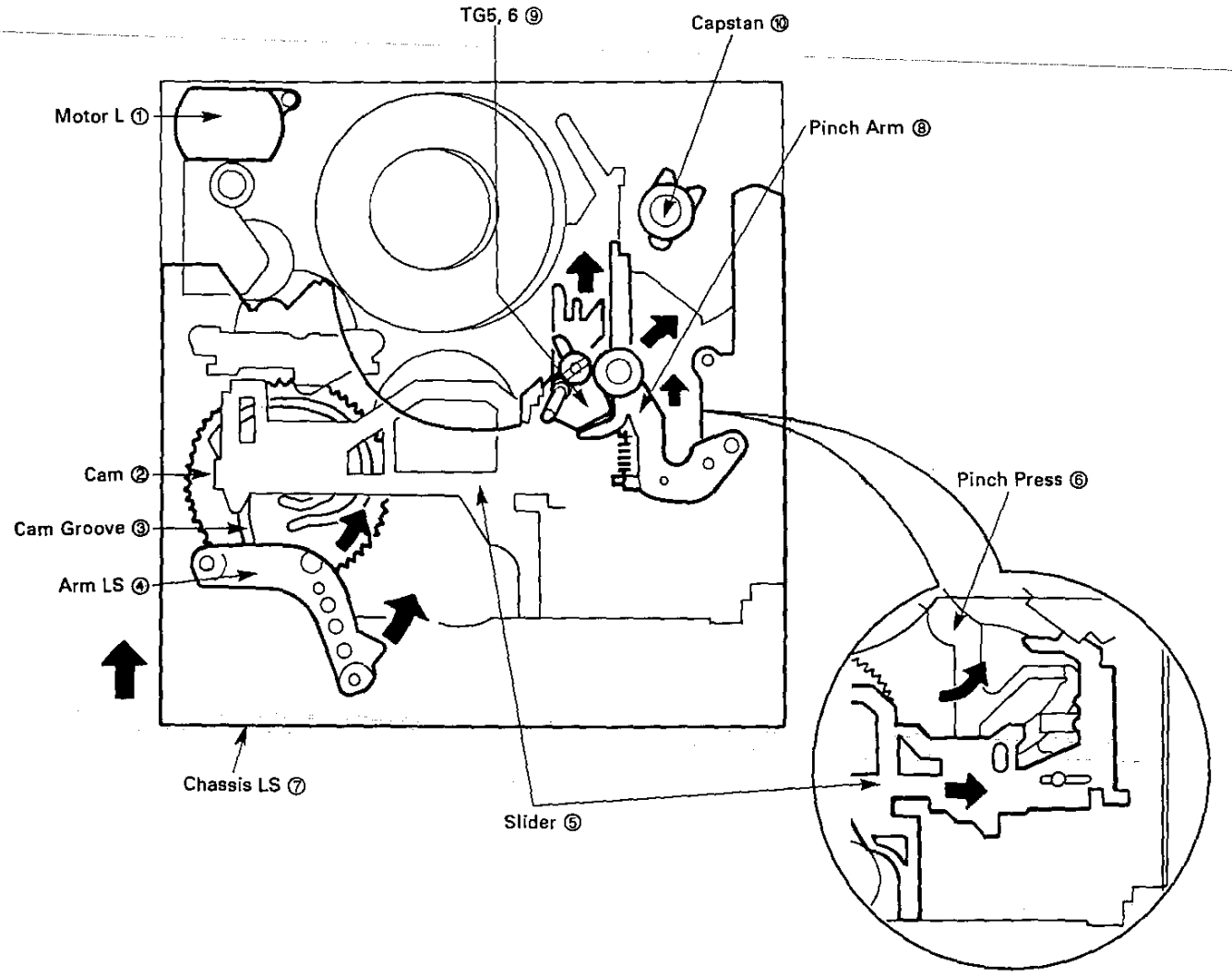
2-4. Arm TG1

Motor L ① rotates.
↓
Chassis LS ⑤ slides.
↓
TG3, TG4 ② slides along the groove of Cam Base TG3, 4 ④.
↓
Arm TG1 ③ moves along TG3, 4 ②.

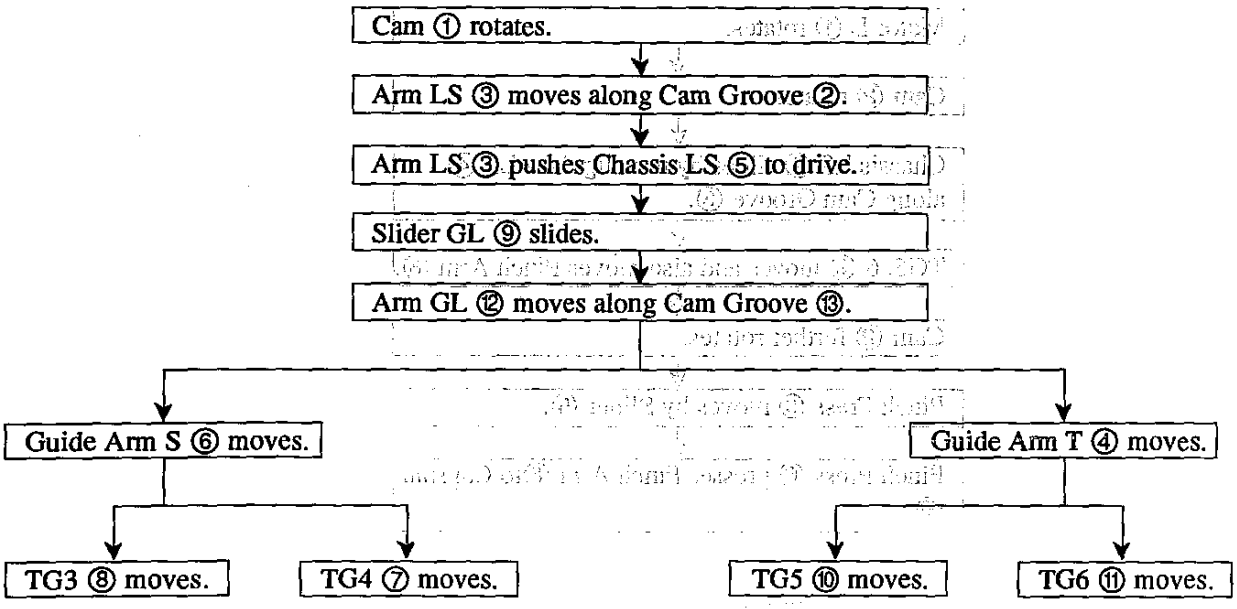


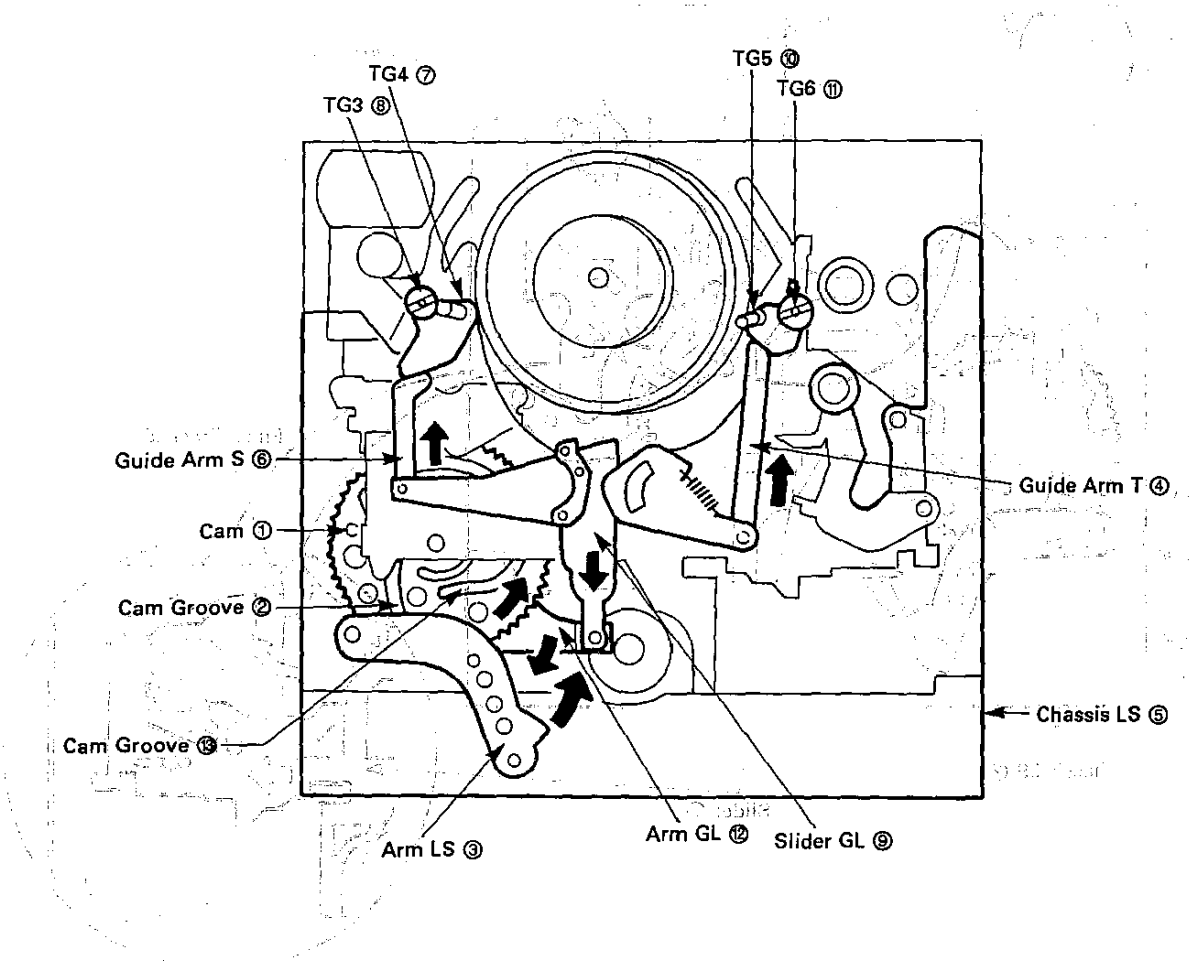
2-5. Pinch Arm (Pinch Roller)

Motor L ① rotates.
↓
Cam ② rotates.
↓
Chassis LS ⑦ slides by moving Arm LS ④ along Cam Groove ③.
↓
TG5, 6 ⑨ moves and also moves Pinch Arm ⑧.
↓
Cam ② further rotates.
↓
Pinch Press ⑥ moves by Slider ⑤.
↓
Pinch Press ⑥ presses Pinch Arm ⑧to Capstan ⑩.



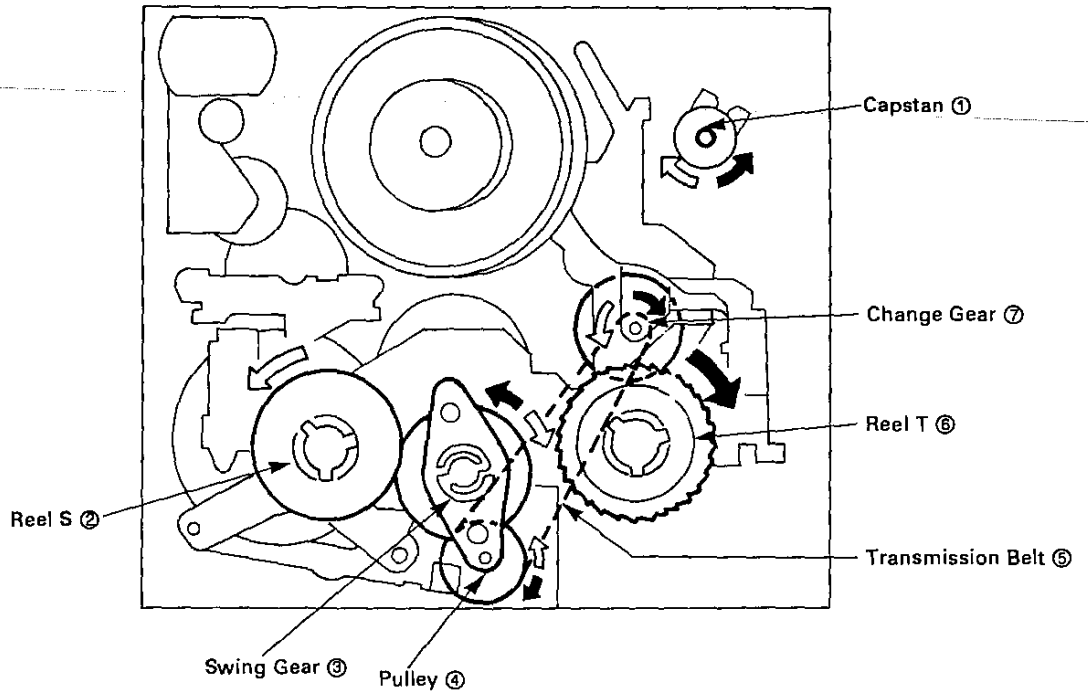
2-6. TG3, 4 and TG5, 6 Bases





2-7. Driving of the Reel Unit

Capstan ① rotates.
↓
PRM is decreased by Change Gear ⑦.
↓
Pulley ④ is rotated by Transmission Belt ⑤.
↓
Swing Gear Arm ③ moves and engages with Reel T ⑥ or S ②.
↓
Reel T ⑥ or S ②rotates.



3. DESCRIPTION ON OPERATION OF THE MECHANISM IN EACH MODE TRANSITION

3-1. Cassette IN (1)

Cassette is put in.

Cassette Control Pawl ① releases locking of Cassette Lid. Thus, Cassette Lid can freely be closed and opened.

Cassette Control ③ is pushed in Arrow A direction.

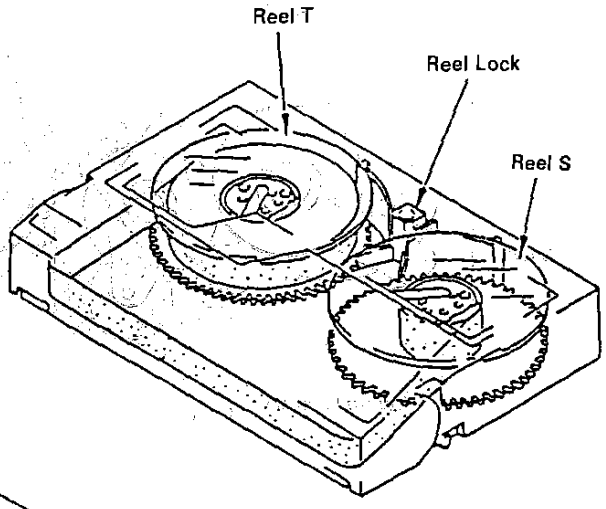
Lock guide ④ moves in Arrow B direction.

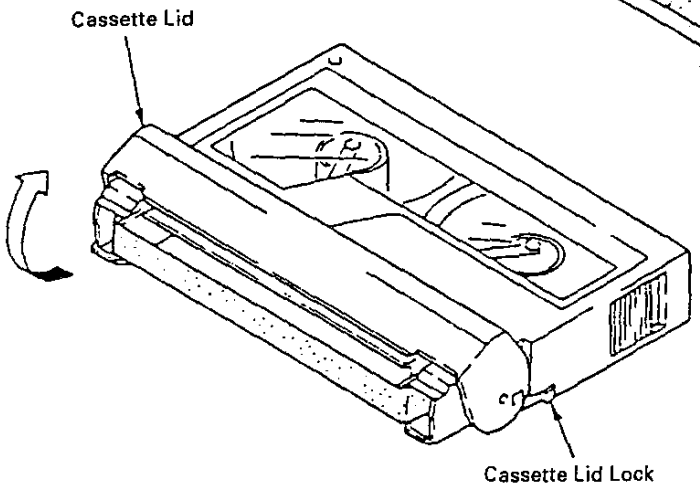
Cassette Lid opens. At the same time, locking of Reel in cassette is reset making Tape removable.

Leaf SW ② is turned ON by Lever Eject ⑤.

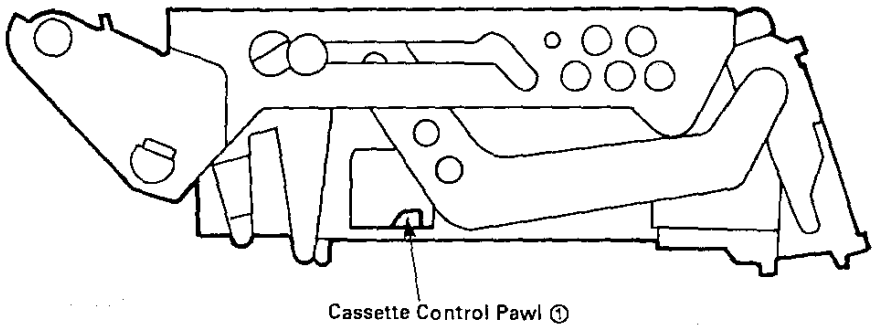
Cassette Control ③ is locked.

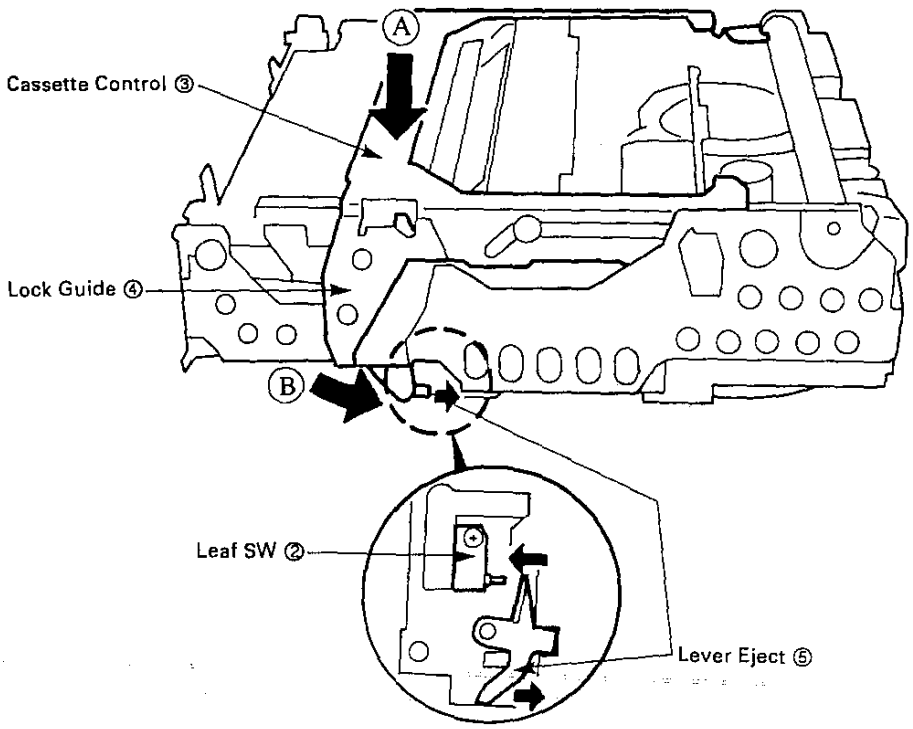
Ⓐ



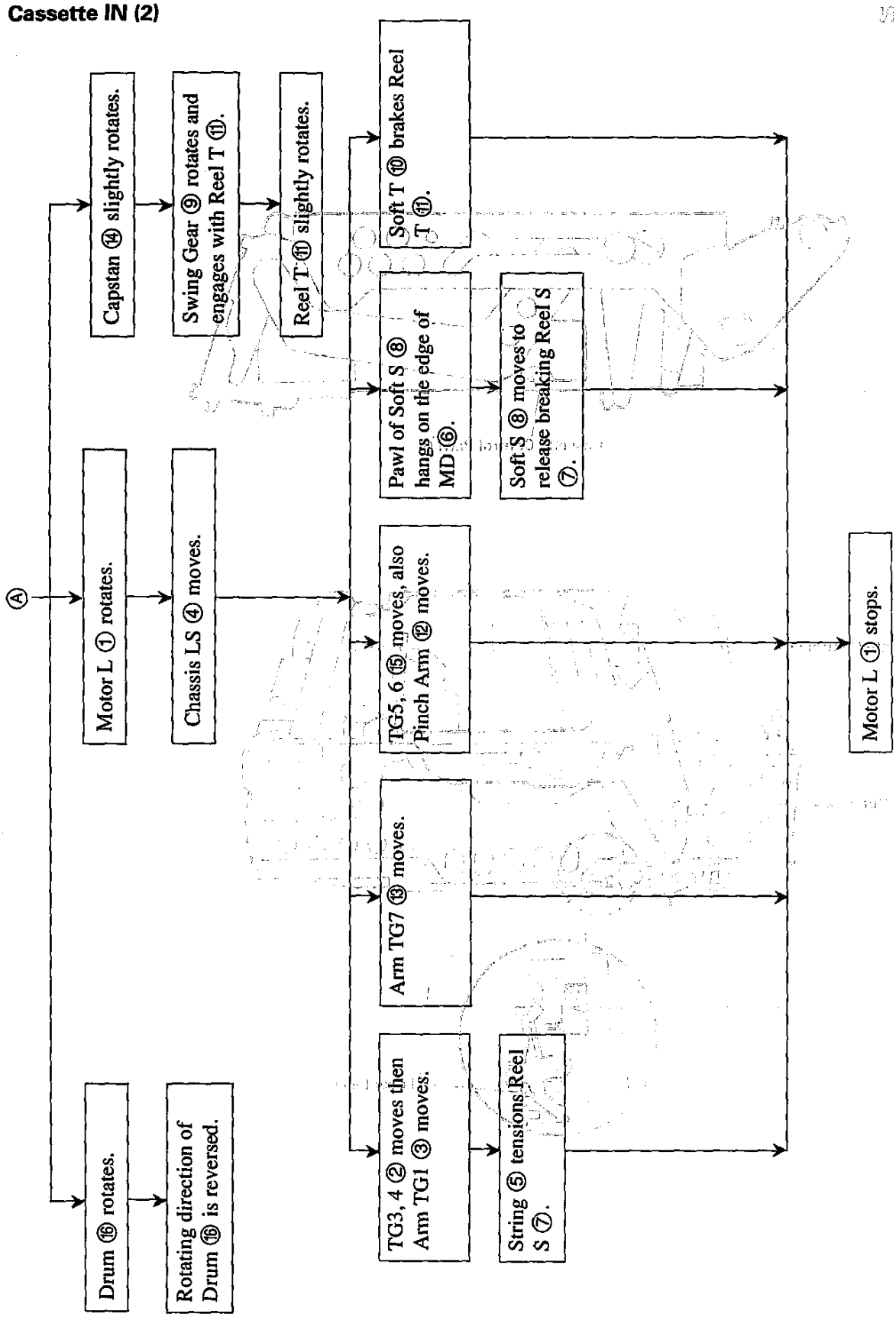


Cassette IN

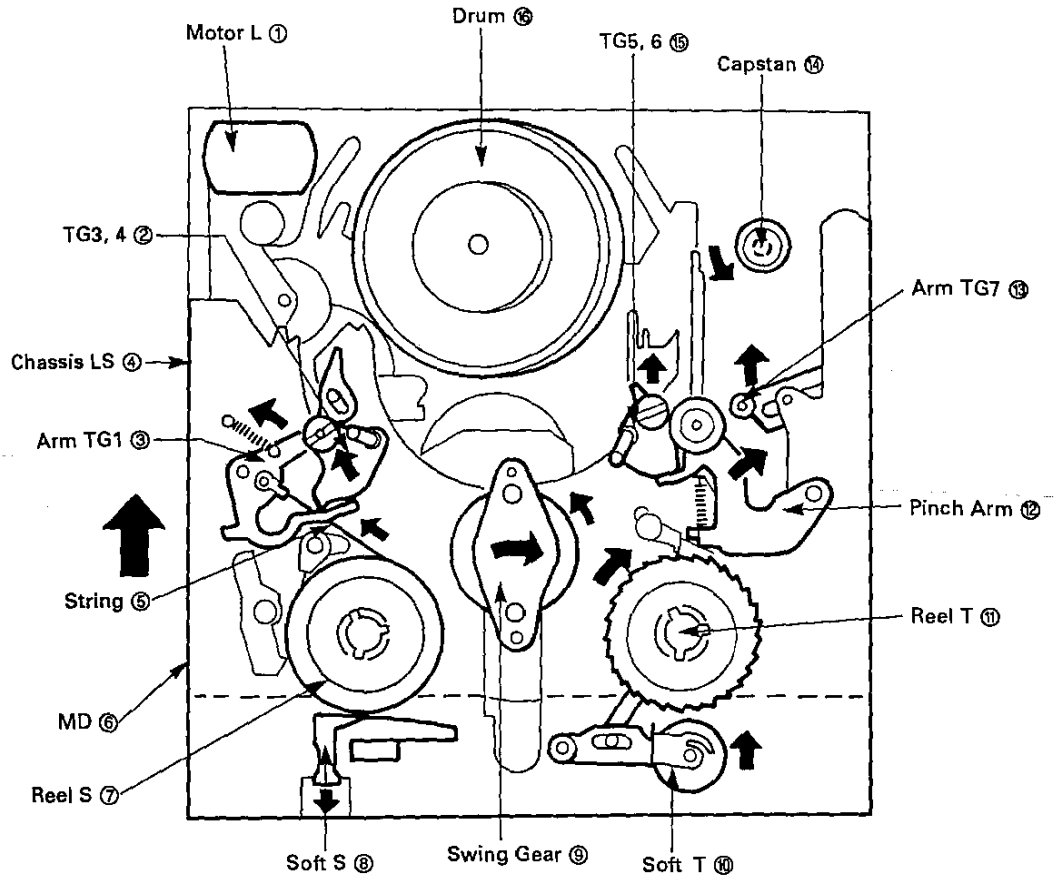

Cassette Control Pawl ①


A
Cassette Control ③
Lock Guide ④
B
Leaf SW ②
Lever Eject ⑤

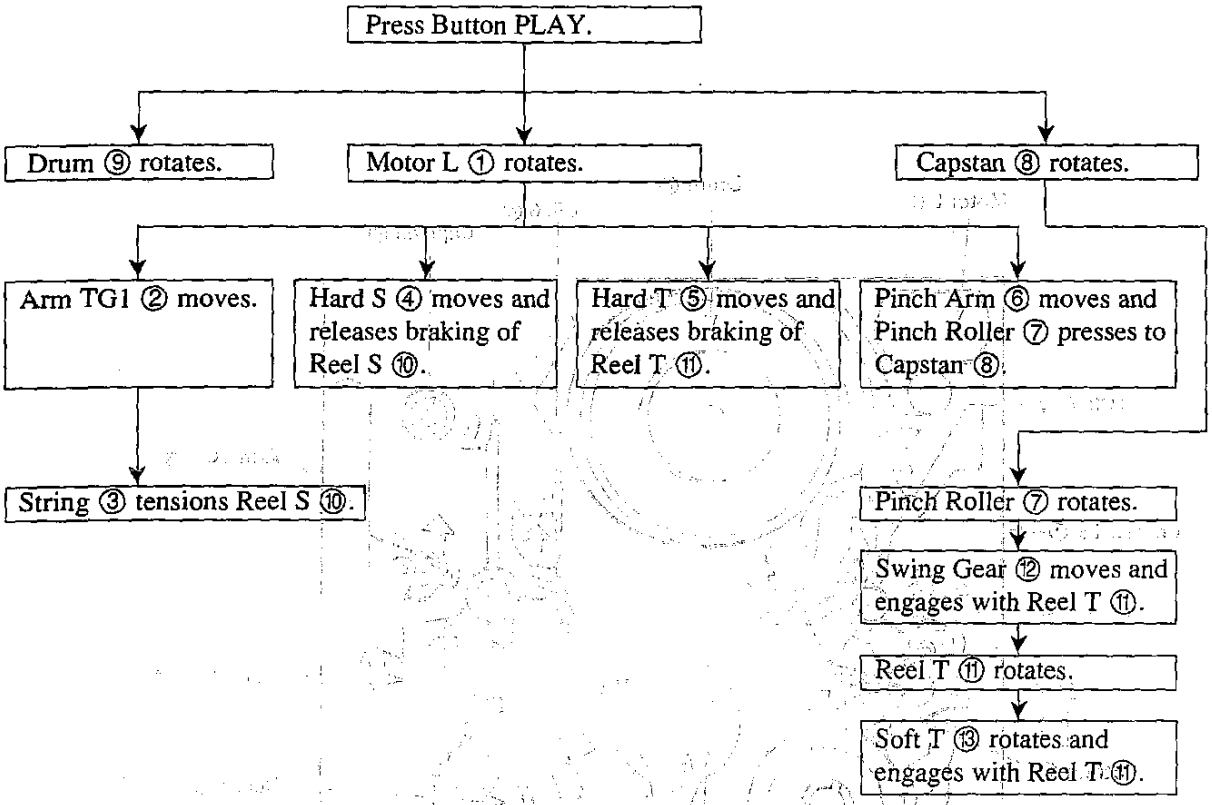
Cassette IN (2)

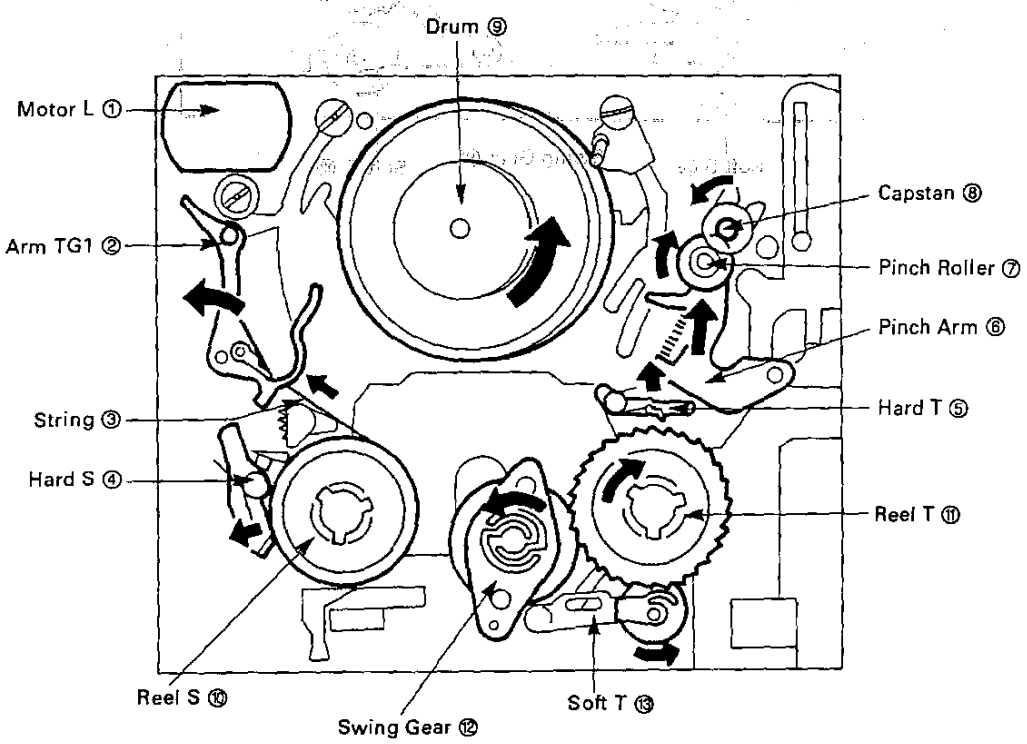


Cassette IN


Motor L ①
Drum ⑯
TG5, 6 ⑮
Capstan ⑭
TG3, 4 ②
Arm TG7 ⑬
Chassis LS ④
Arm TG1 ③
Pinch Arm ⑫
String ⑤
Reel T ⑪
MD ⑥
Reel S ⑦
Soft S ⑧
Swing Gear ⑨
Soft T ⑩

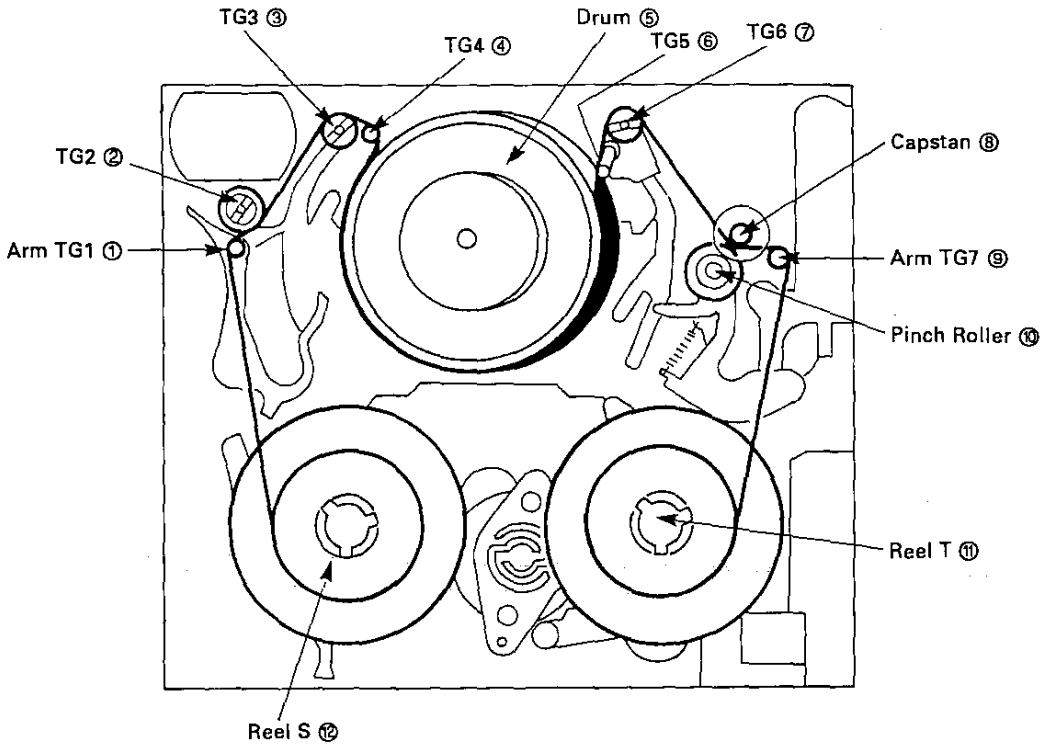
3-2. PLAY


Press Button PLAY.
Drum ⑨ rotates.
Motor L ① rotates.
Capstan ⑧ rotates.
Arm TG1 ② moves.
Hard S ④ moves and releases braking of Reel S ⑩.
Hard T ⑤ moves and releases braking of Reel T ⑪.
Pinch Arm ⑥ moves and Pinch Roller ⑦ presses to Capstan ⑧.
String ③ tensions Reel S ⑩.
Pinch Roller ⑦ rotates.
Swing Gear ⑫ moves and engages with Reel T ⑪.
Reel T ⑪ rotates.
Soft T ⑬ rotates and engages with Reel T ⑪.


Drum ⑨
Motor L ①
Arm TG1 ②
String ③
Hard S ④
Capstan ⑧
Pinch Roller ⑦
Pinch Arm ⑥
Hard T ⑤
Reel T ⑪
Reel S ⑩
Swing Gear ⑫
Soft T ⑬

3-3. TAPE PATH

Tape is pulled out of Reel S ⑫.
↓
Tape is tensioned by Arm TG1 ①.
↓
Tape passes TG2 ②.
↓
Tape passes TG3 ③ and direction of tape is changed by TG4 ④.
↓
Tape wraps on Drum ⑤.
↓
Tape is directed back by TG5 ⑥.
↓
Tape passes TG6 ⑦.
↓
Tape passes between pressed Capstan ⑧ and pinch Roller ⑩.
↓
Tape passes Arm TG7 ⑨.
↓
Tape is reeled up on Reel T ⑪.



3-4. PLAY → PAUSE

Press Button PAUSE during PLAY.

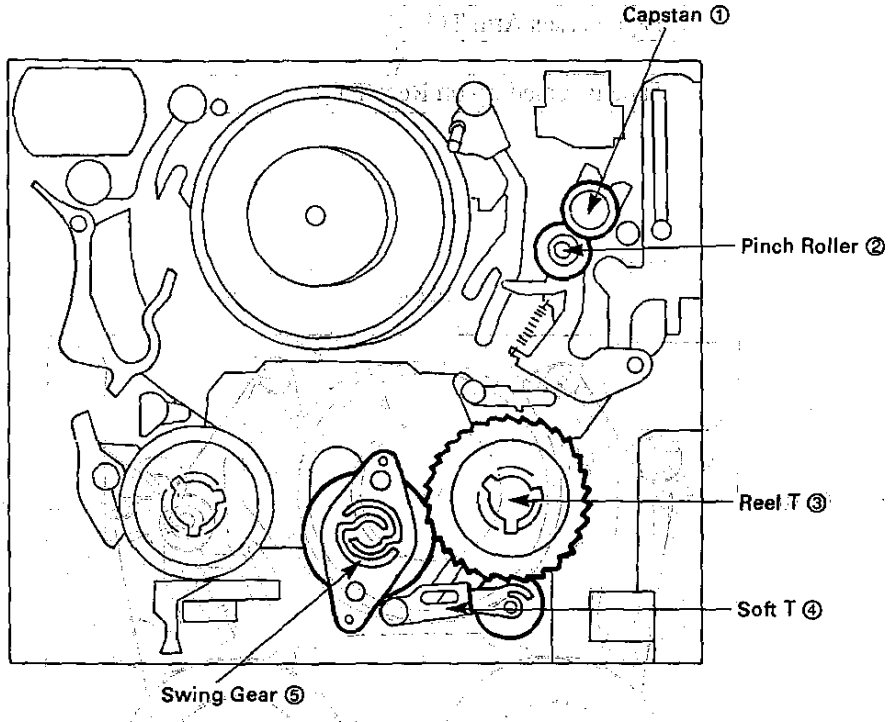
Capstan ① stops.

Swing Gear ⑤ stops.

Pinch Roller ② stops.

Reel T ③ stops.

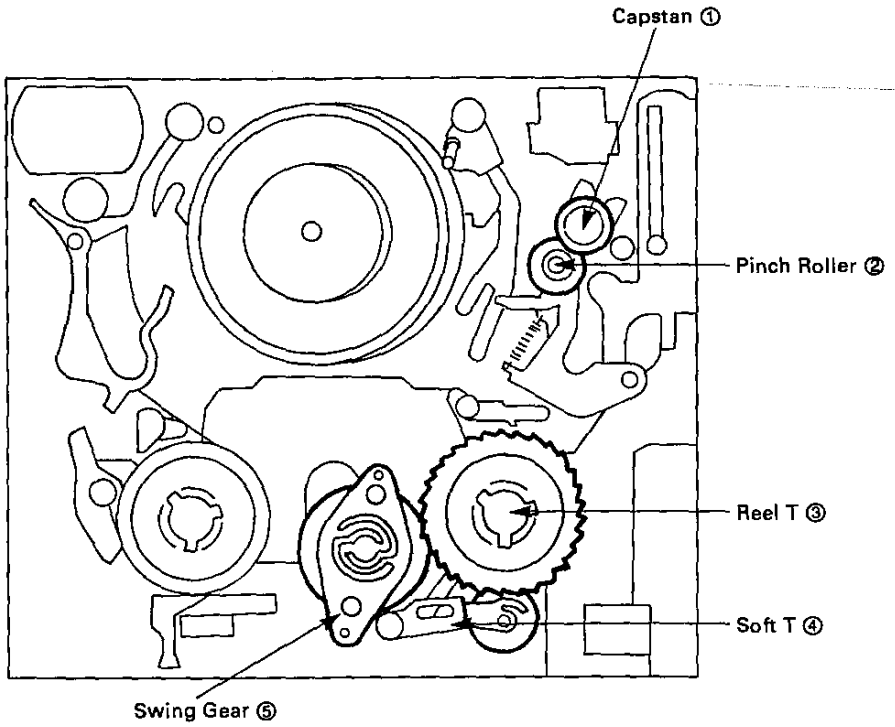
Soft T ④ stops.



3-5. PLAY → CUE

Press Button FF during PLAY.
↓
Capstan ① rotates in high frequency.
↓
Swing Gear ⑤ rotates in high frequency.
↓
Reel T ③ rotates in high frequency.
↓
Soft T ④ rotates in high frequency.

Pinch Roller ② rotates in high frequency.



3-6. PLAY → REW

Press Button REW during PLAY.

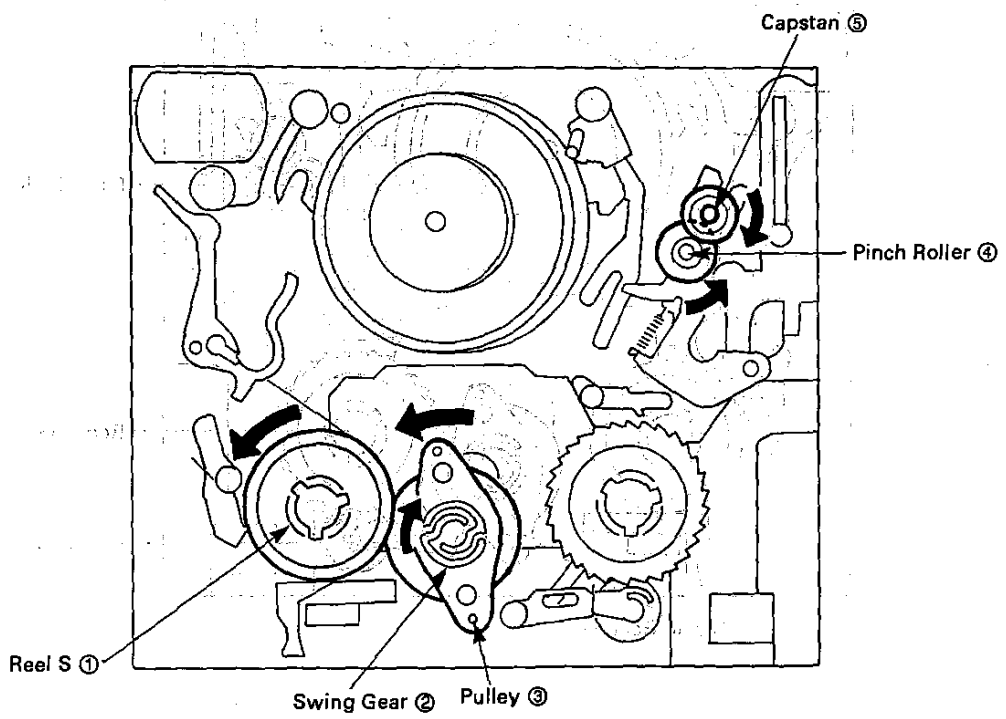
Capstan ⑤ reversely rotates in high frequency.

Pinch Roller ④ reversely rotates in high frequency.

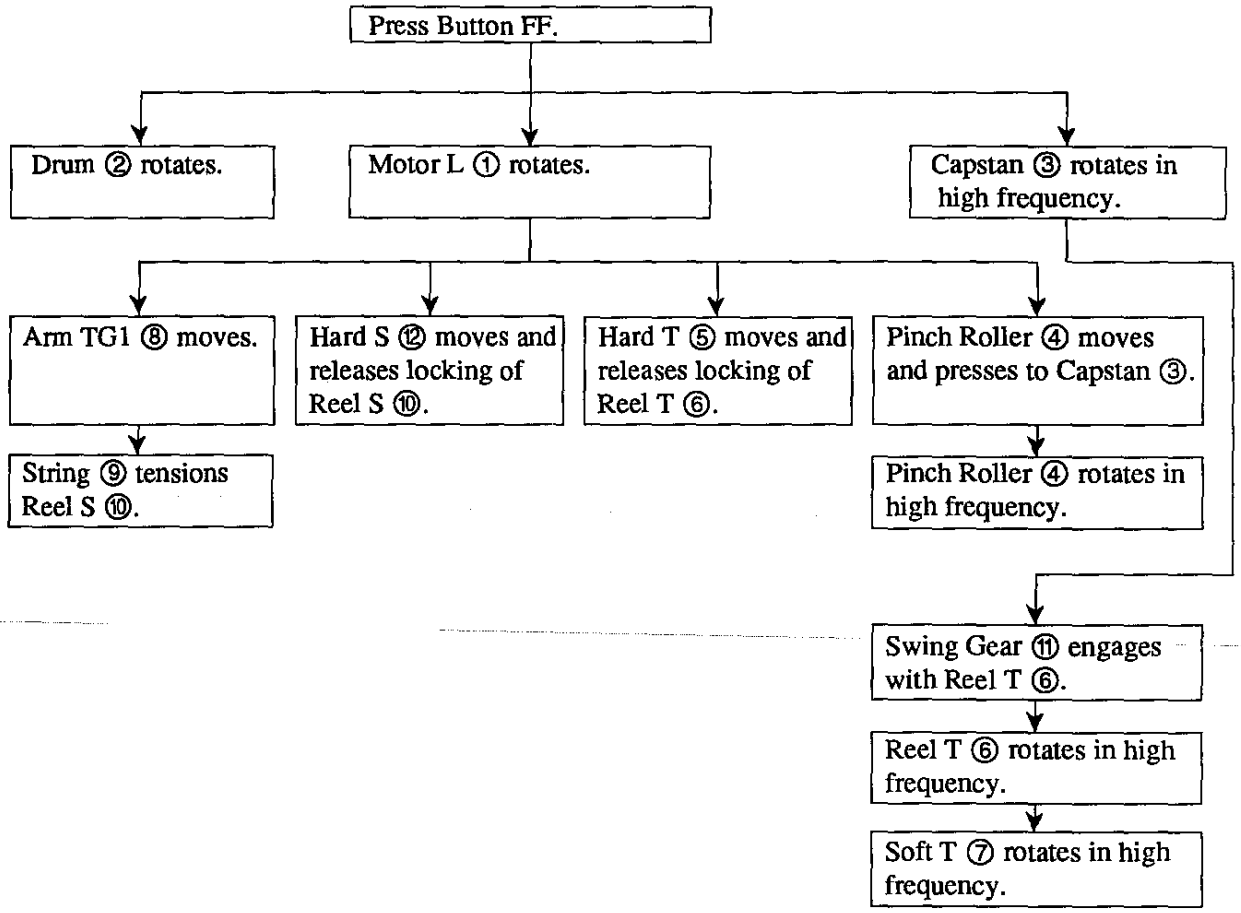
Pulley ③ reversely rotates in high frequency.

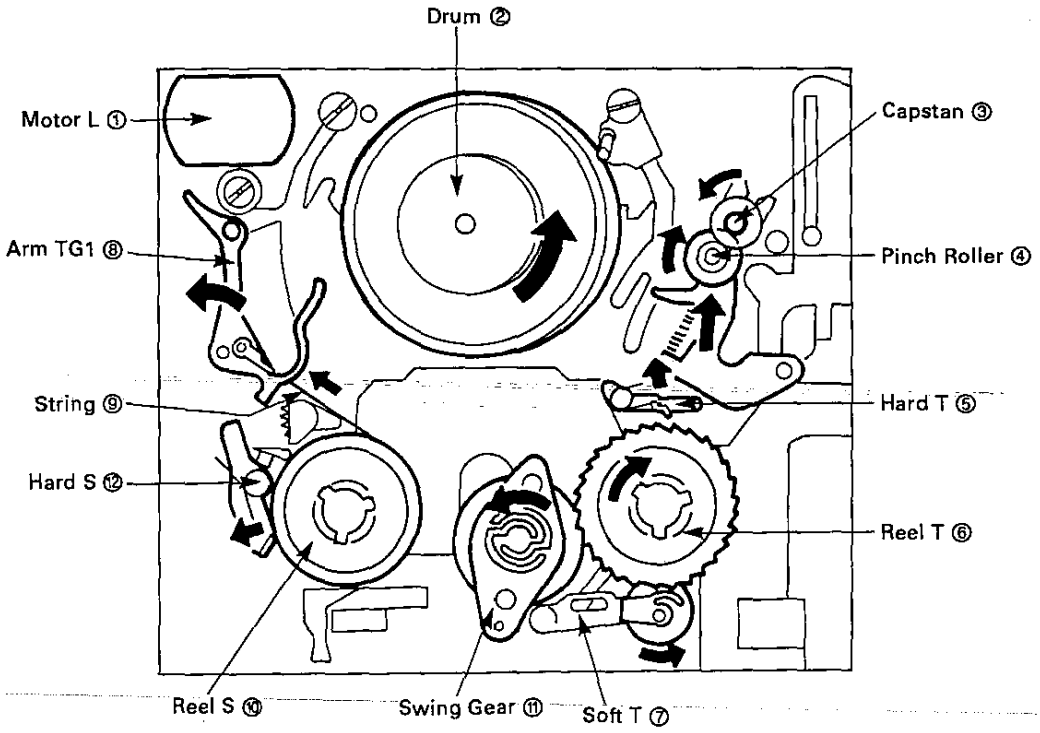
Swing Gear ② engages with Reel S ①.

Reel S ① rotates in high frequency.

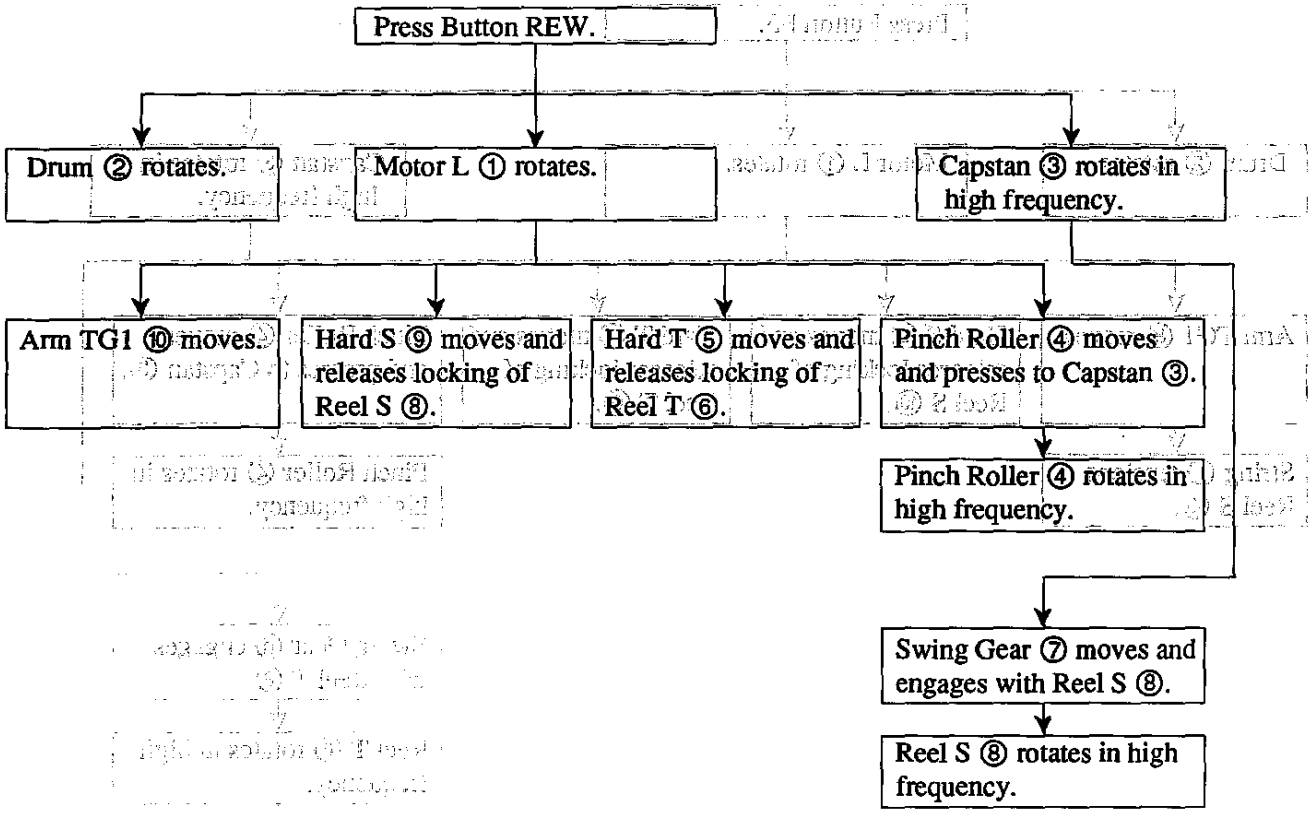


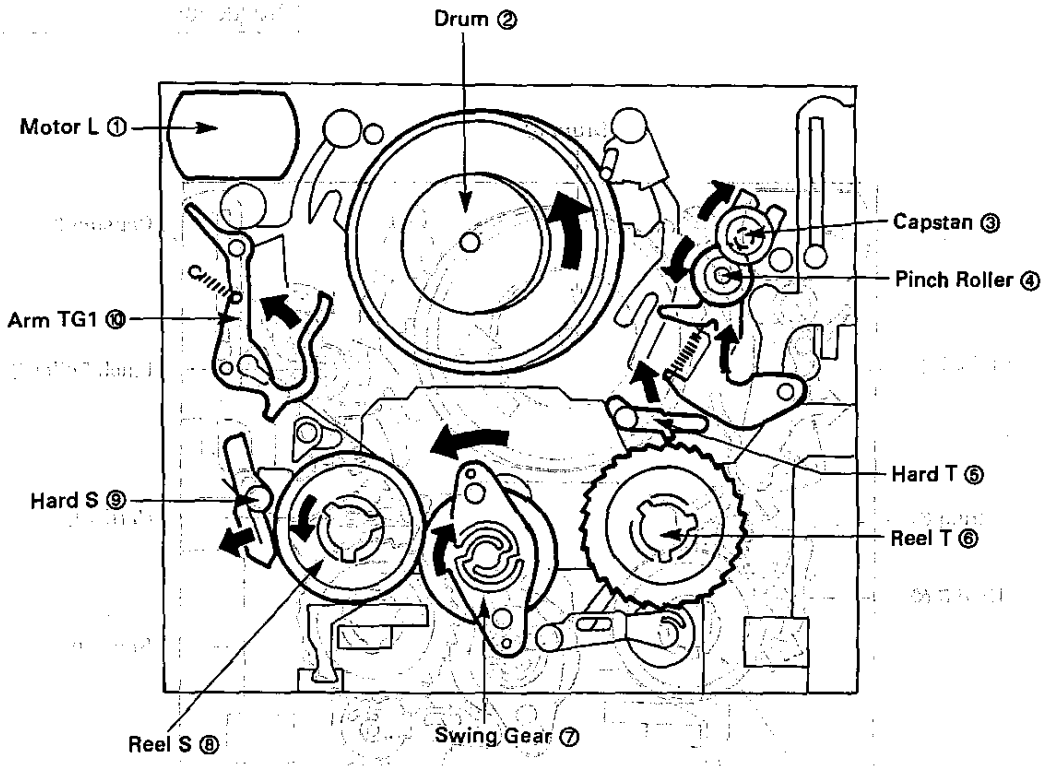
3-7. FF


Press Button FF.
Drum ② rotates.
Motor L ① rotates.
Capstan ③ rotates in high frequency.
Arm TG1 ⑧ moves.
Hard S ⑫ moves and releases locking of Reel S ⑩.
Hard T ⑤ moves and releases locking of Reel T ⑥.
Pinch Roller ④ moves and presses to Capstan ③.
String ⑨ tensions Reel S ⑩.
Pinch Roller ④ rotates in high frequency.
Swing Gear ⑪ engages with Reel T ⑥.
Reel T ⑥ rotates in high frequency.
Soft T ⑦ rotates in high frequency.

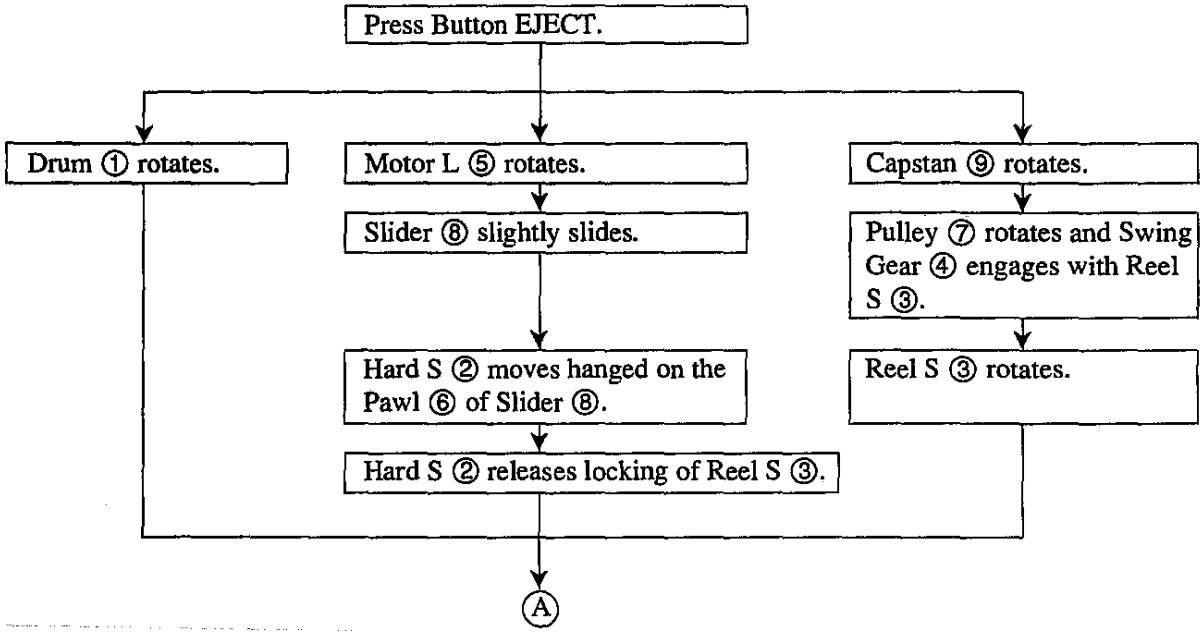

Drum ②
Motor L ①
Capstan ③
Arm TG1 ⑧
Pinch Roller ④
String ⑨
Hard T ⑤
Hard S ⑫
Reel T ⑥
Reel S ⑩
Swing Gear ⑪
Soft T ⑦

3-8. REW

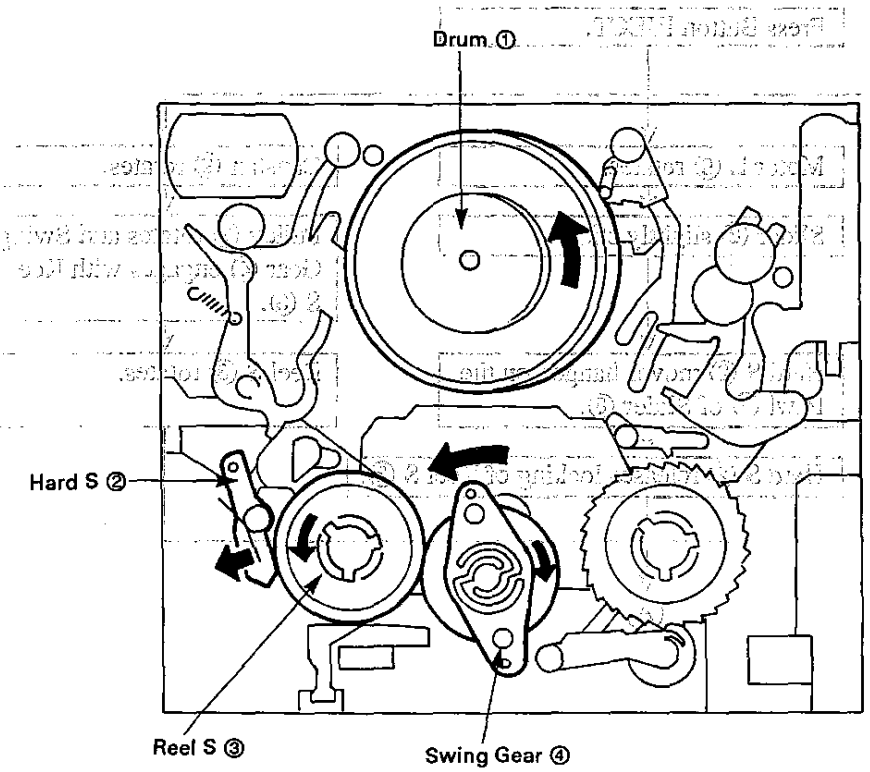

Press Button REW.
Drum ② rotates.
Motor L ① rotates.
Capstan ③ rotates in high frequency.
Arm TG1 ⑩ moves.
Hard S ⑨ moves and releases locking of Reel S ⑧.
Hard T ⑤ moves and releases locking of Reel T ⑥.
Pinch Roller ④ moves and presses to Capstan ③.
Pinch Roller ④ rotates in high frequency.
Swing Gear ⑦ moves and engages with Reel S ⑧.
Reel S ⑧ rotates in high frequency.

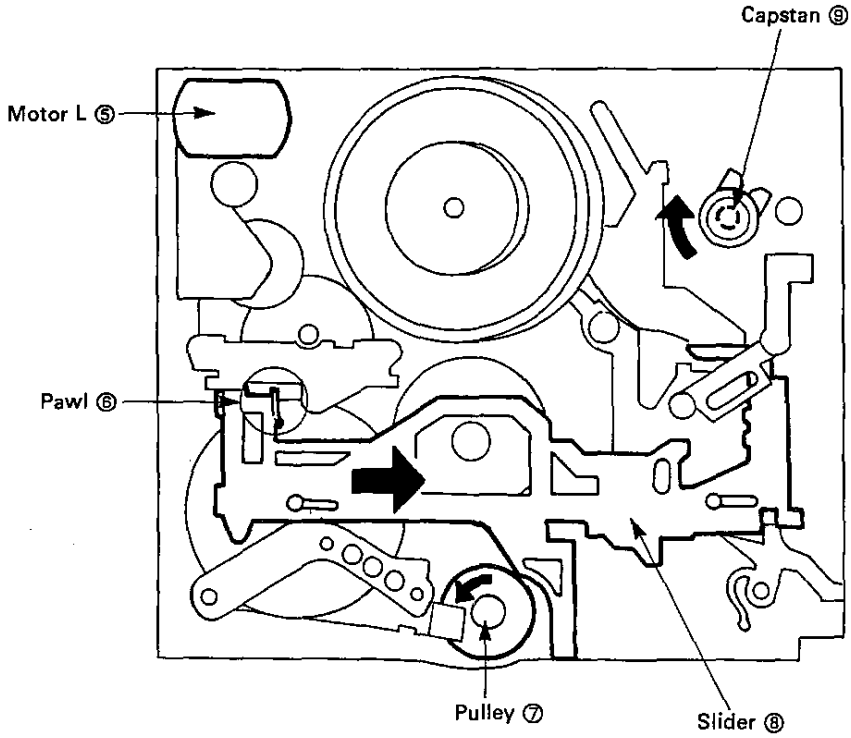

Drum ②
Motor L ①
Capstan ③
Pinch Roller ④
Arm TG1 ⑩
Hard T ⑤
Hard S ⑨
Reel T ⑥
Reel S ⑧
Swing Gear ⑦

3-9. EJECT (1)

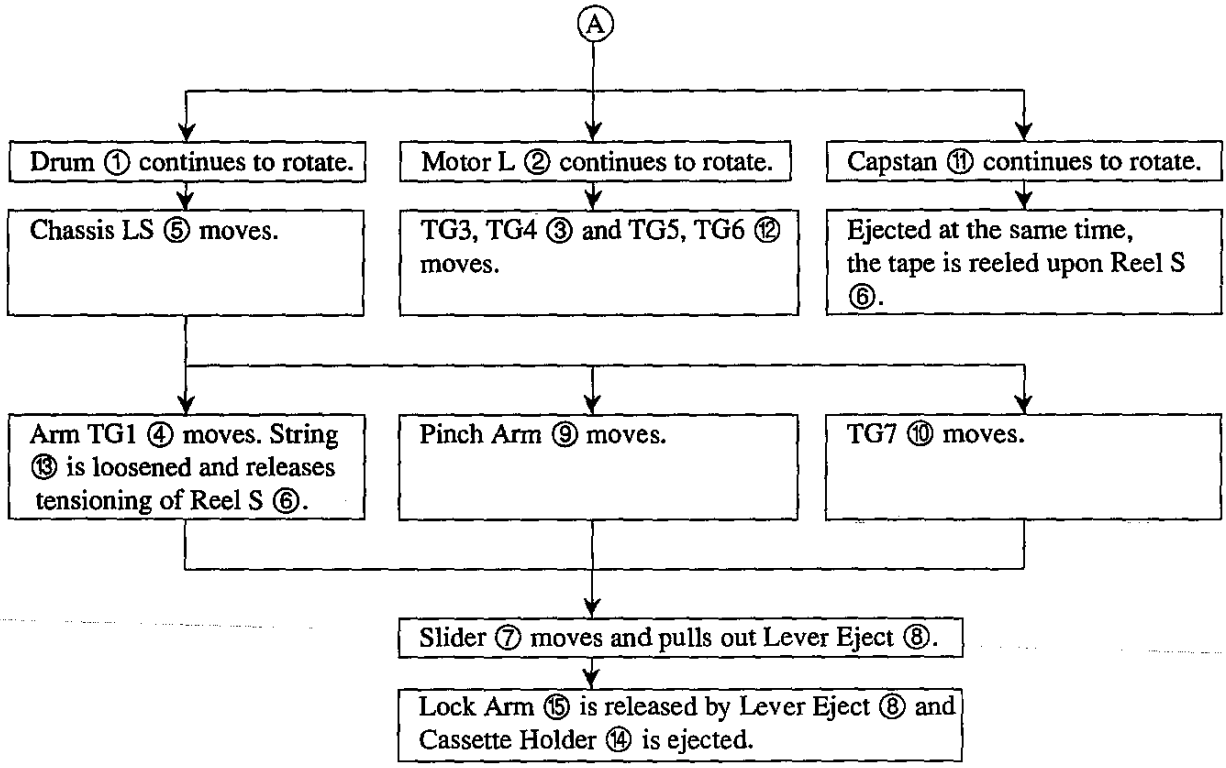

Press Button EJECT.
Drum ① rotates.
Motor L ⑤ rotates.
Capstan ⑨ rotates.
Slider ⑧ slightly slides.
Pulley ⑦ rotates and Swing Gear ④ engages with Reel S ③.
Hard S ② moves hanged on the Pawl ⑥ of Slider ⑧.
Reel S ③ rotates.
Hard S ② releases locking of Reel S ③.
A

EJECT (1)

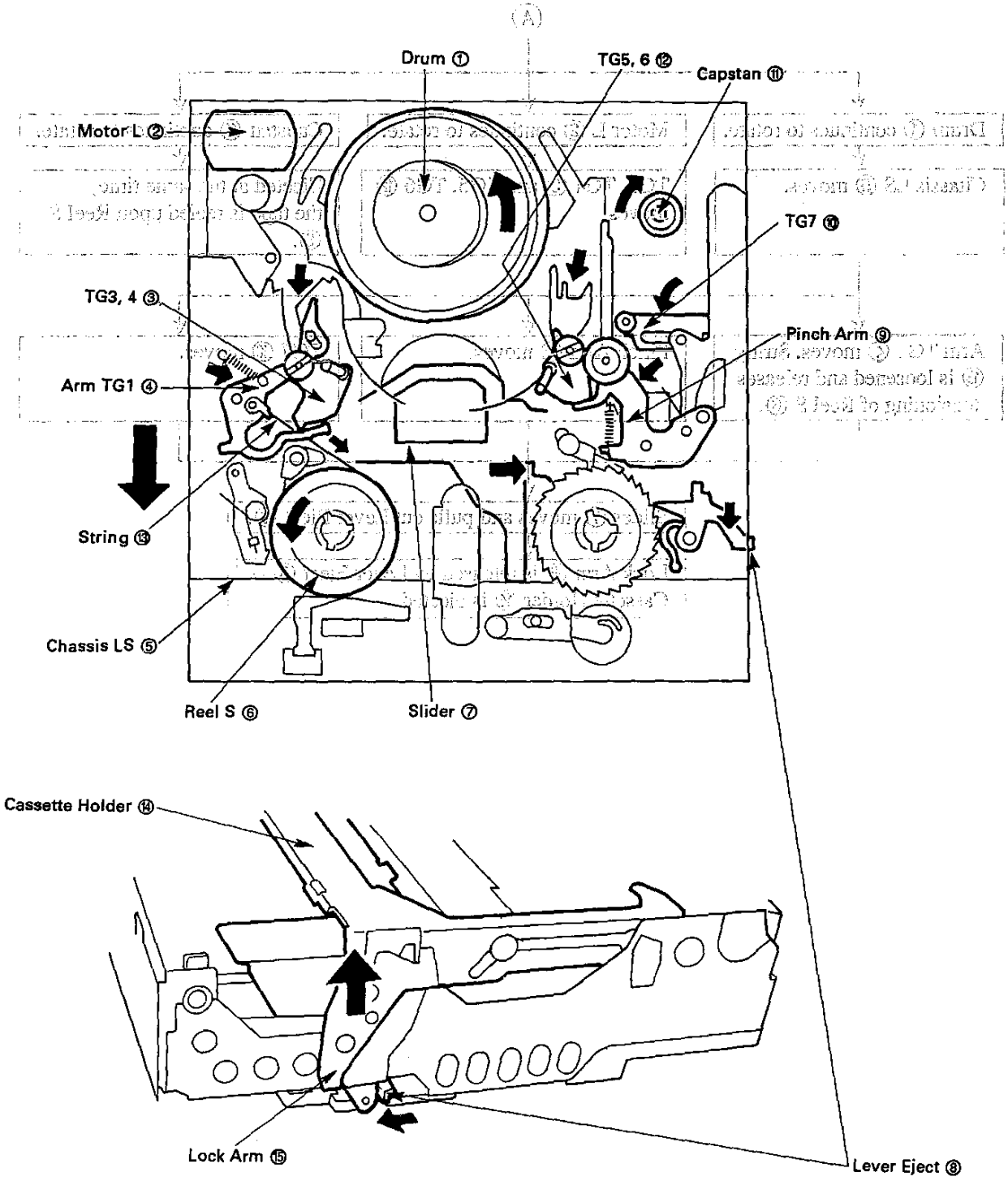

Drum ①
Hard S ②
Reel S ③
Swing Gear ④


Capstan ⑨
Motor L ⑤
Pawl ⑥
Pulley ⑦
Slider ⑧

EJECT (2)


Ⓐ
Drum ① continues to rotate.
Motor L ② continues to rotate.
Capstan ⑪ continues to rotate.
Chassis LS ⑤ moves.
TG3, TG4 ③ and TG5, TG6 ⑫ moves.
Ejected at the same time, the tape is reeled upon Reel S ⑥.
Arm TG1 ④ moves. String ⑬ is loosened and releases tensioning of Reel S ⑥.
Pinch Arm ⑨ moves.
TG7 ⑩ moves.
Slider ⑦ moves and pulls out Lever Eject ⑧.
Lock Arm ⑮ is released by Lever Eject ⑧ and Cassette Holder ⑭ is ejected.

EJECT (2)


Drum ①
TG5, 6 ⑫
Capstan ⑪
Motor L ②
TG7 ⑩
TG3, 4 ③
Pinch Arm ⑨
Arm TG1 ④
String ⑬
Chassis LS ⑤
Reel S ⑥
Slider ⑦
Cassette Holder ⑭
Lock Arm ⑮
Lever Eject ⑧

CAMERA SECTION

4. BLOCK DIAGRAM

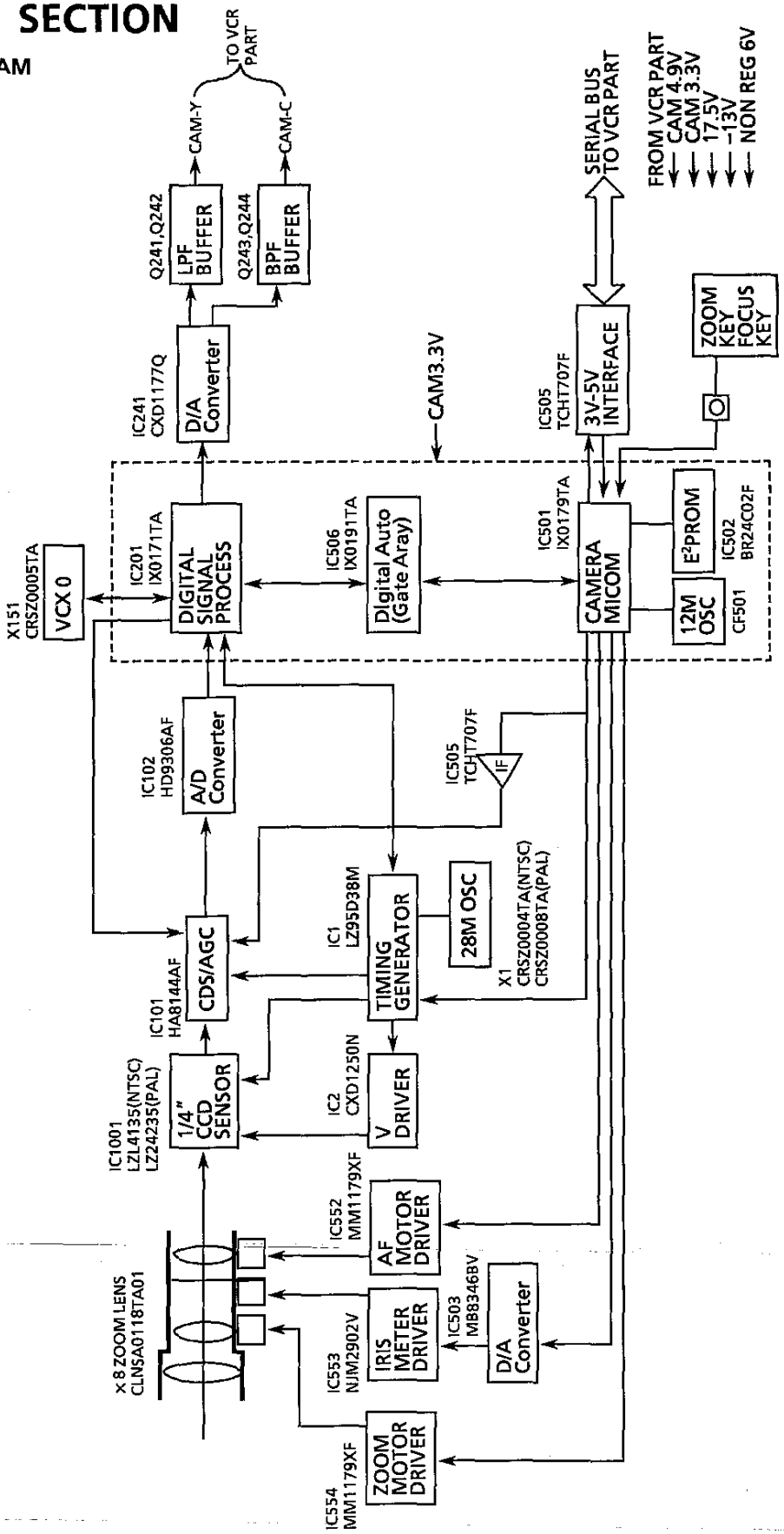


Figure 4-1 CAMERA SECTION BLOCK DIAGRAM

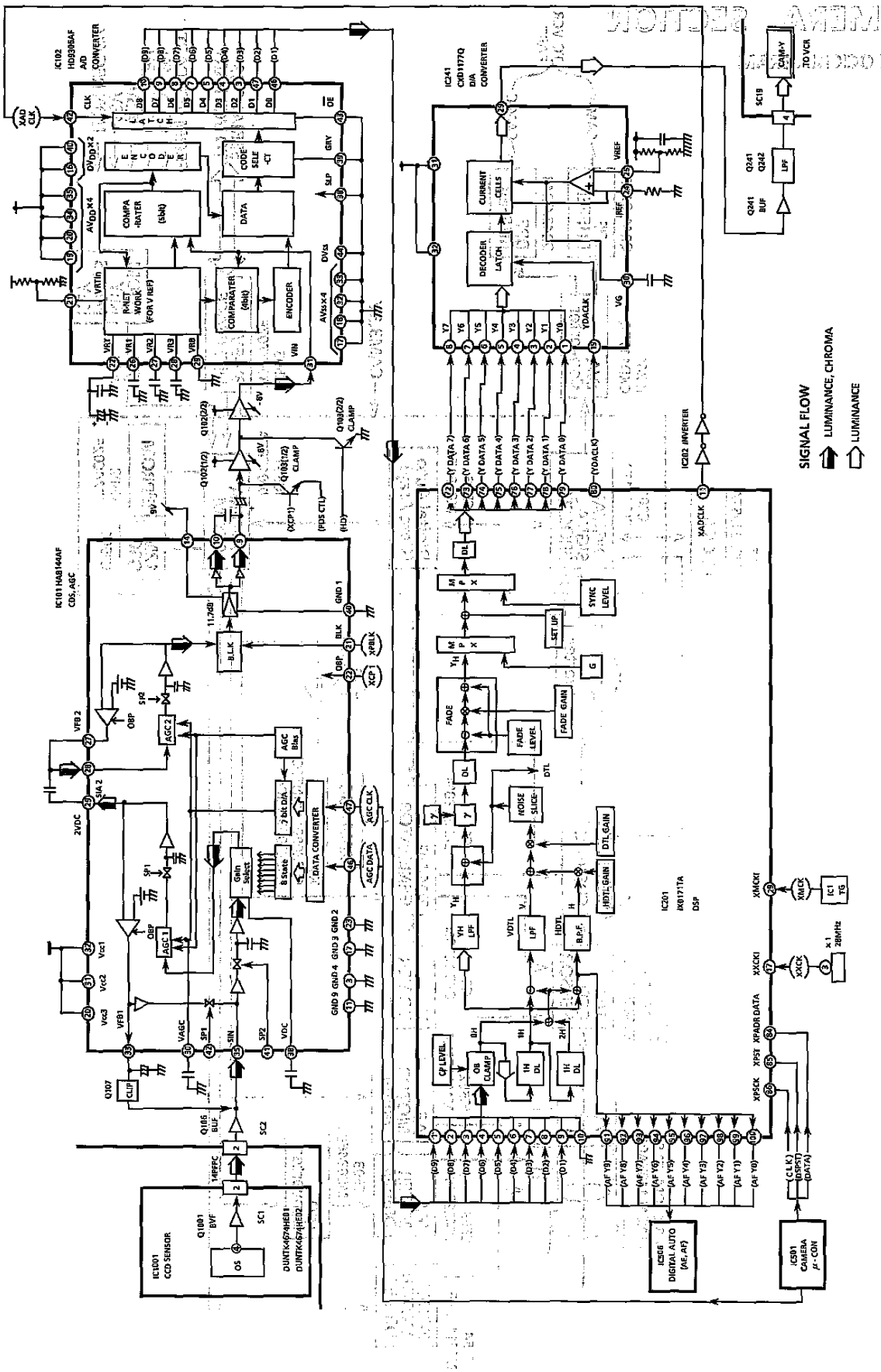


Figure 4-2 CAMERA LUMINANCE BLOCK DIAGRAM

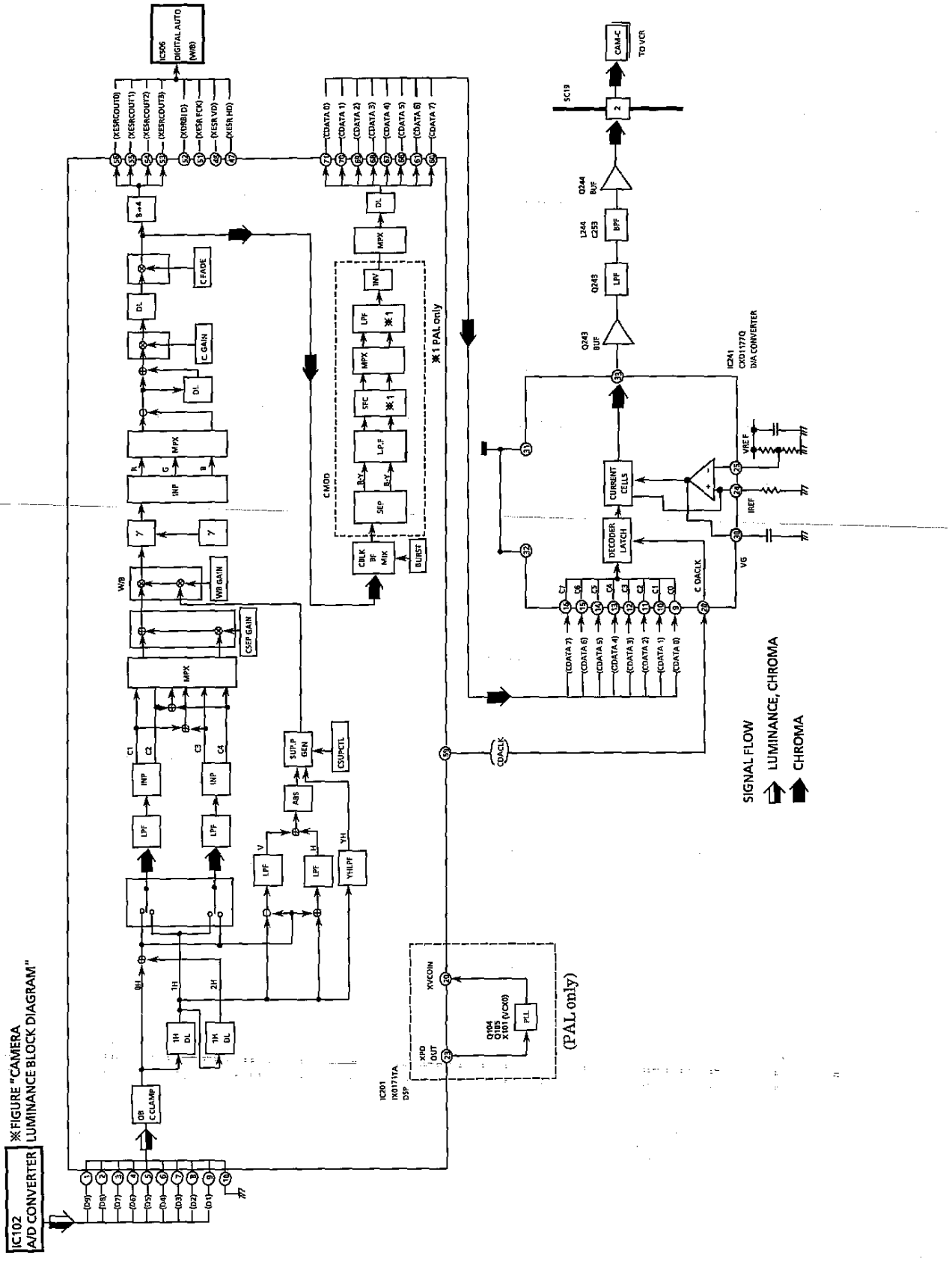


Figure 4-3 CHROMINANCE BLOCK DIAGRAM (VL-E30S/H/X, E7E/D, E30U/C, E35U/E35)

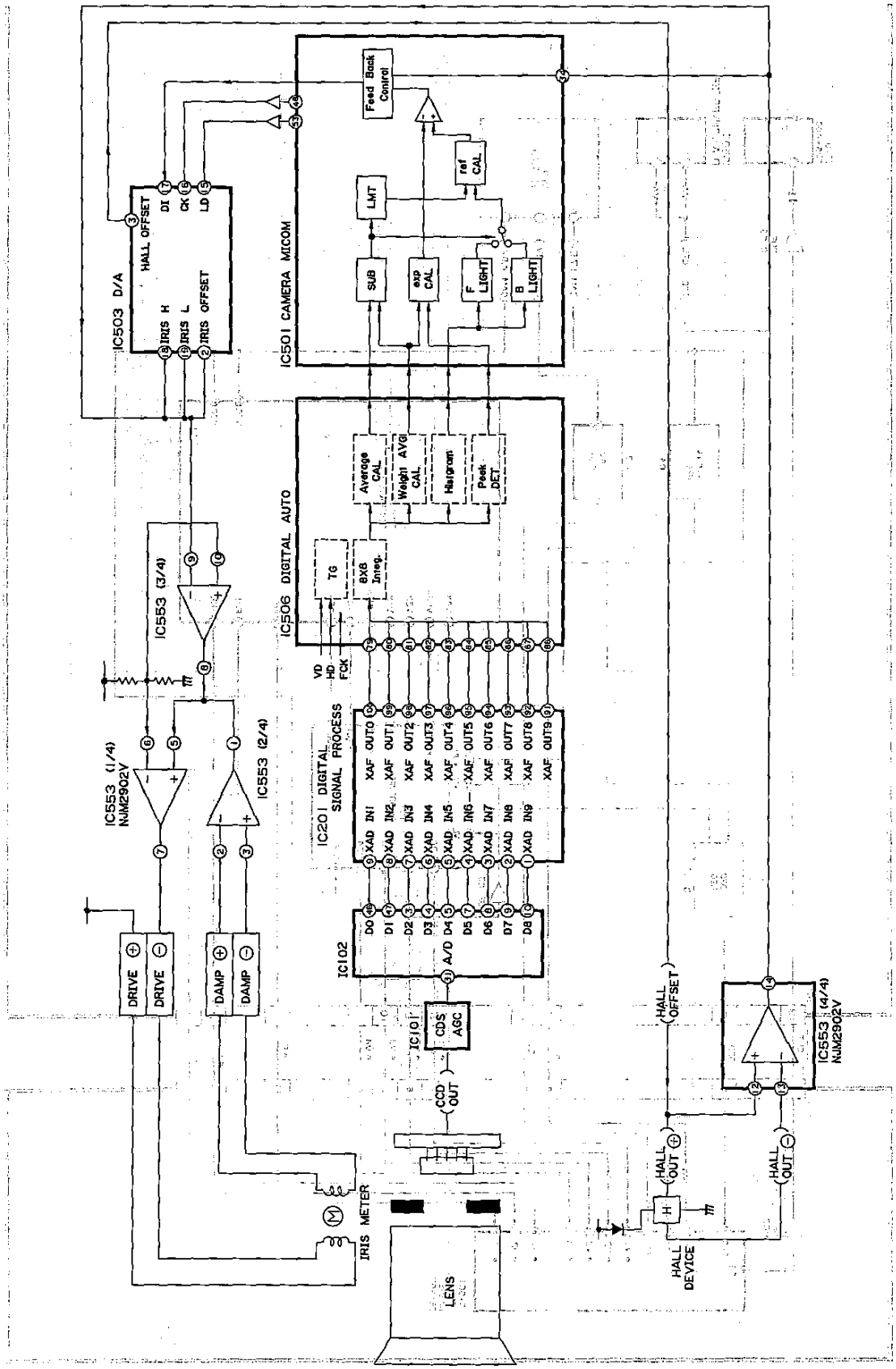


Figure 4-6 IRIS BLOCK DIAGRAM

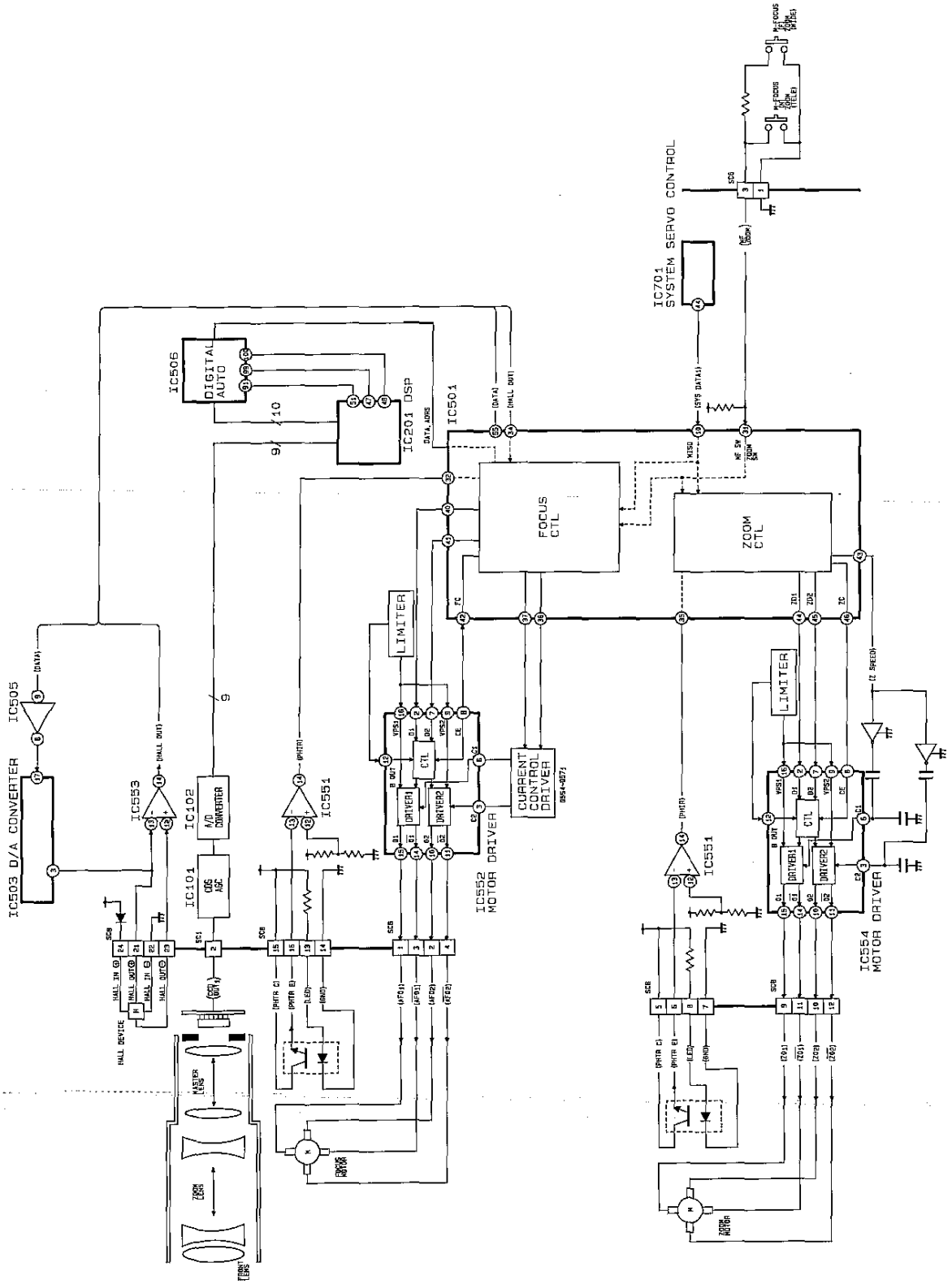


Figure 4-7 AUTO FOCUS/ZOOM SECTION BLOCK DIAGRAM

MEMO

5. CCD OPERATION (LZ24235) (VL-E30S/H/X/E7E/D, E40S/H/X/E8E/D)

5-1. Outline and features

The cameras use a is 1/4" solid state CCD that has 320,000 picture elements (effective 290,000). Figure 5-1 shows the composition of these picture elements.

The CCD is an inter-line system with field accumulation employing a complementary mosaic color filter.

The camera is equipped with V-OFD (vertical type overflow drain) high speed shutter, which requires no memory device.

(Shutter modes: 1/50 and 1/500 (sports mode))

The major features are:

- 1/4" 542(H) × 582(V) Approx. 320,000 picture elements
  (Effective picture elements: 512(H) × 582(V) Approx. 290,000)
- Blooming suppression
- Variable electronic shutter function (2 modes in this model)

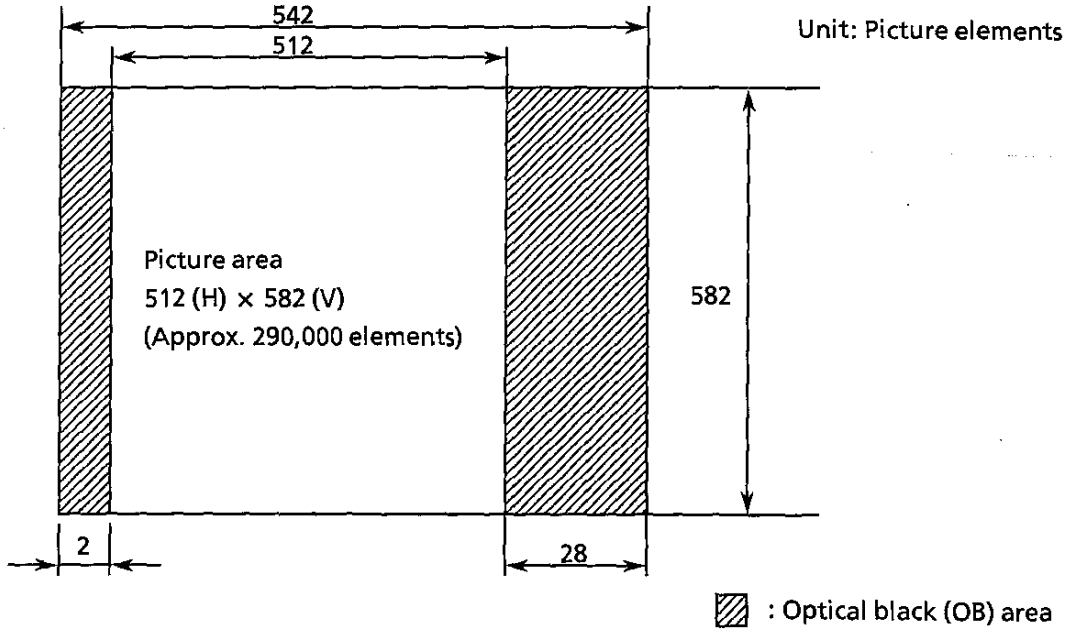


Figure 5-1. Picture Elements Composition

5-2. Basic operation of a CCD camera

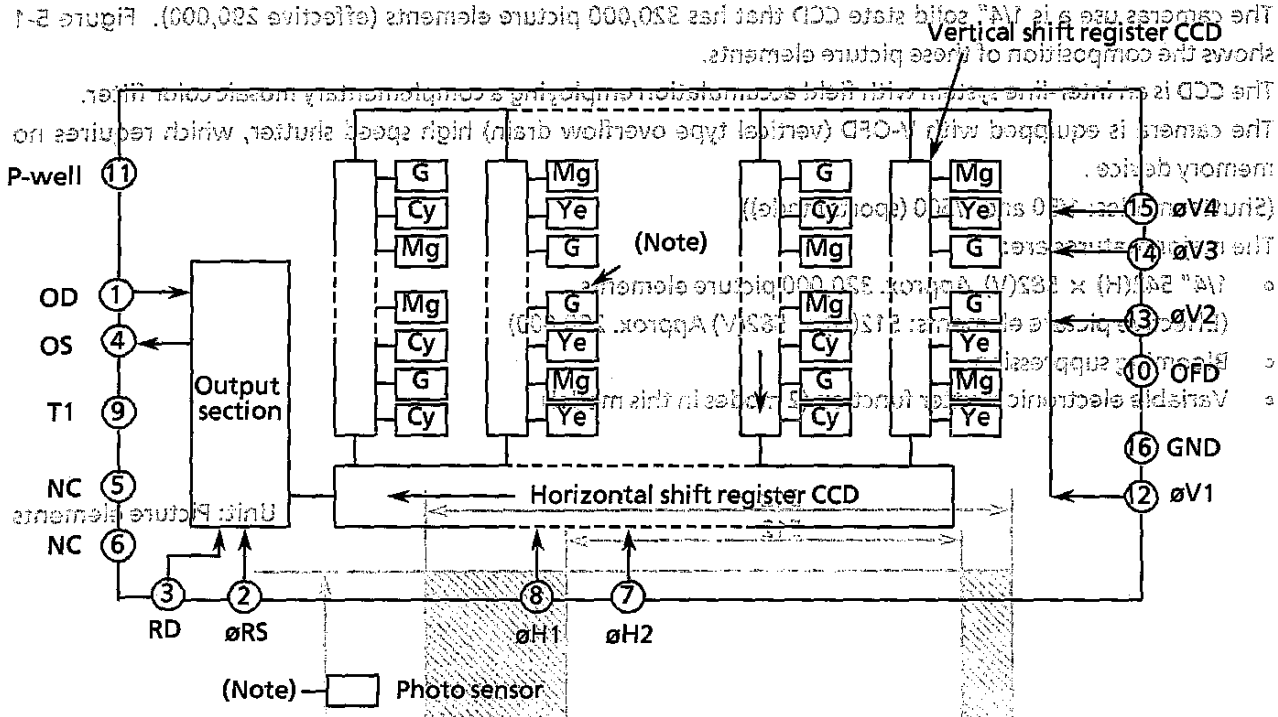


Figure 5-2. Internal Block Diagram

- Refer to Figure 5-2. When the photo sensor receives light, an electric charge corresponding to its intensity will be produced and stored.
- The charge is then sent out to the vertical shift register during the vertical blanking period by the sensor's charge read-out pulses SG1 and SG2, which are overlaid on the vertical transfer clock signals øV1 and øV3.
- The signal charge read out to the vertical shift register is transferred to the horizontal shift register by the vertical register transfer clock signals øV1 ~ øV4. This is done step by step for every horizontal blanking period.
- The signal charge transferred to the horizontal shift register is then sent to the output section by the horizontal register transfer clock signals øH1 and øH2 within the horizontal scan time (1H: 64 µsec), covering the number of horizontal elements.
- In the output section, the charge detection capacitor, which is initialized by the reset gate clock signal øRS, receives its charge from the horizontal shift register and outputs the electric potential corresponding to the charges received. This electric potential is amplified by the output amplifier to produce CCD signal .

5-3. High speed shutter operation

The CCD image sensor adopted in this model enableds the draining of unnecessary charge in every horizontal scan during the horizontal blanking period, enhancing the high speed electronic shutter operation. Thus, while having no memory section for the high speed shutter operation, various shutter modes have been made available.

① V-OFD (Vertical overflow drain)

As shown in Figure 5-3 (a), Vsub voltage is applied to the n-substrate during normal operation, suppressing the generation of excessive charge which will cause smearing or blooming.

When the electronic shutter is operated, Δ Vsub voltage is added to drain the charge accumulated in the sensor output of the substrate. (Figure 5-3 (b))

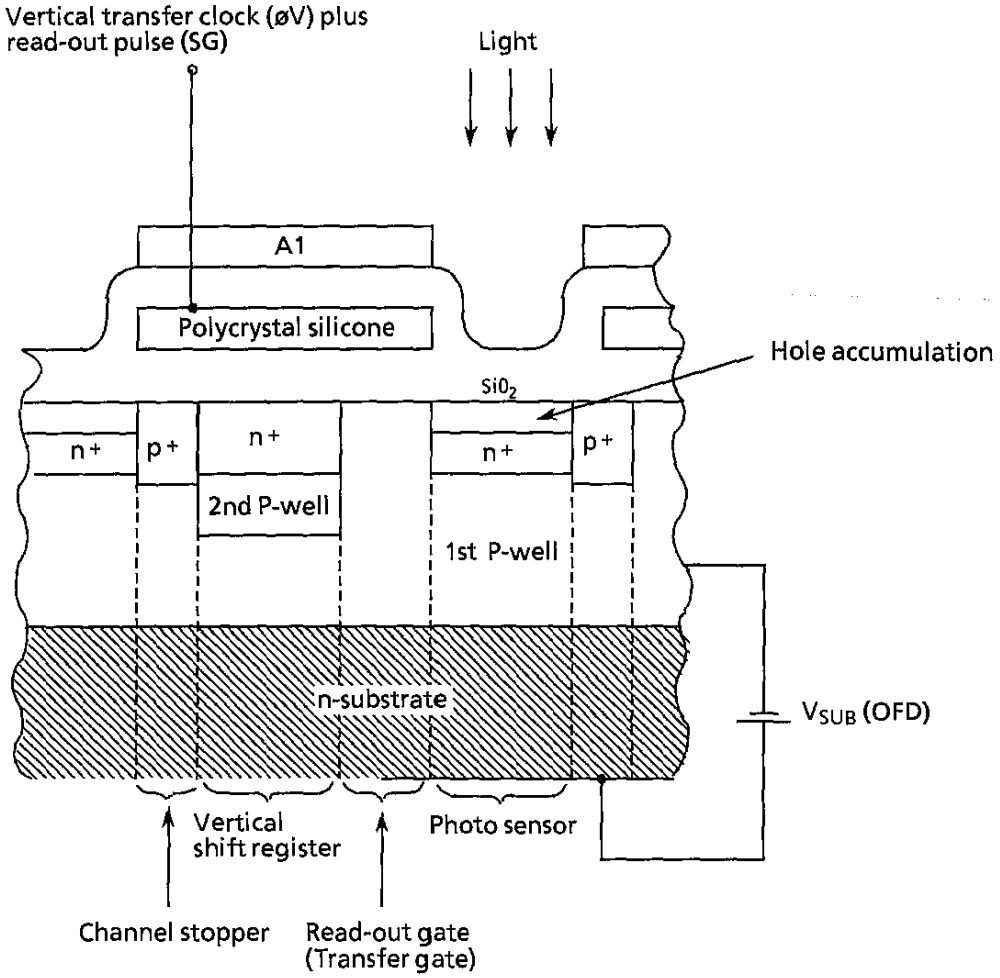


Figure 5-3 (a). Sectional View of CCD Image Sensor

Smearing: When the sensor receives intensive light, the generated charge leaks out to the vertical register. This appears as vertical white lines in the picture.

Blooming: When there is a single extremely bright spot in the picture, the charge from the photo sensor will fill up the transfer gate and the channel stopper. As a result, the light appears to surround the bright spot.

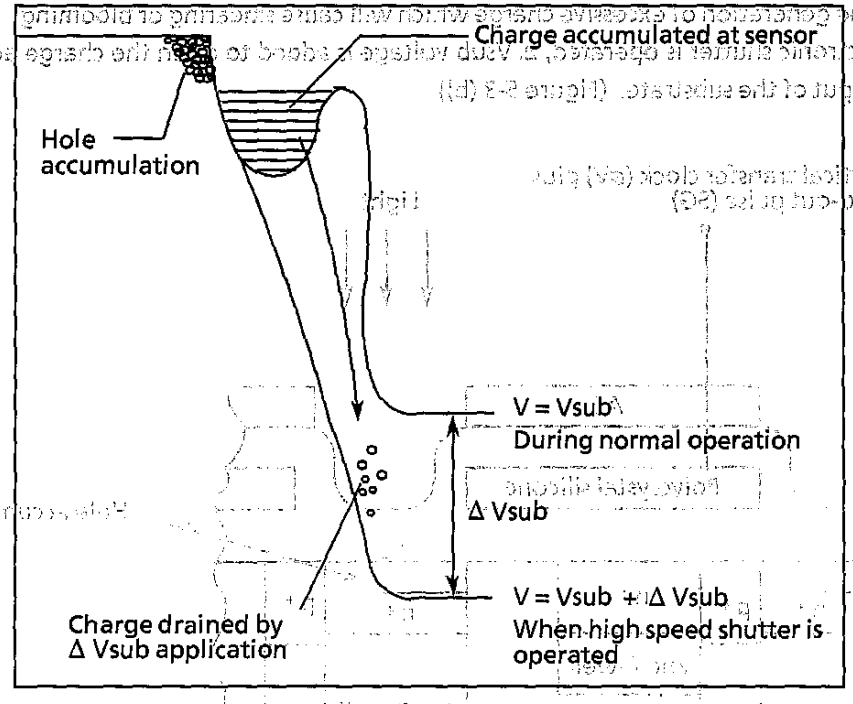


Figure 5-3 (b). Vertical Potential Distribution at Sensor Section

② Shutter pulse timing

Figure 5-4 shows the timing chart between OFD (pin ⑩ of the CCD image sensor) and øV1 pulse (pin ⑫ of CCD image sensor) in each shutter speed. Figure 5-4 indicates that, after the sensor read-out, the exposure time (charge accumulation time) for the following read-out can be varied by the number of ΔVsub pulses following the sensor read-out pulse.

In this model, pin ㉑(OFDX) of IC1 (CCD timing generator) sends out ΔVsub pulse corresponding to the preset shutter speed, which is supplied to pin ② of IC2 (V-driver). After being amplified in IC2, the pulse is sent out from pin ⑲(Vsub) of IC2. It is then overlaid on the OFD voltage and supplied to pin ⑩ of the CCD image sensor (IC1001).

Refer to Chapter (4 Circuits Description) for details of shutter speed setting.

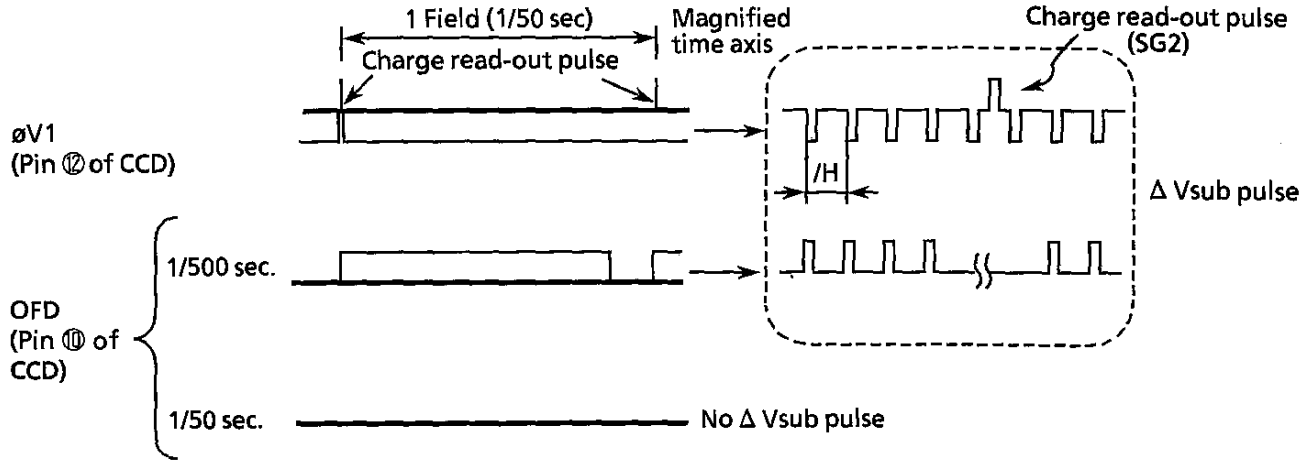


Figure 5-4. Timing Chart for Each Shutter Speed

5-4. Drive pulse timing

① Vertical drive (4-phase drive)

Due to the arrangement of the color mosaic filter, the read-out is made by changing the pulse timing of øV1, øV2, øV3 and øV4 at the start of the 1.3 field and 2.4 field. During the normal transfer, the drive frequency is 15.625 KHz.

Figure 5-5 and Figure 5-6 show the timing charts for vertical transfer and charge read-out respectively.

⑤ Electronic shutter (1/2000 sec.)

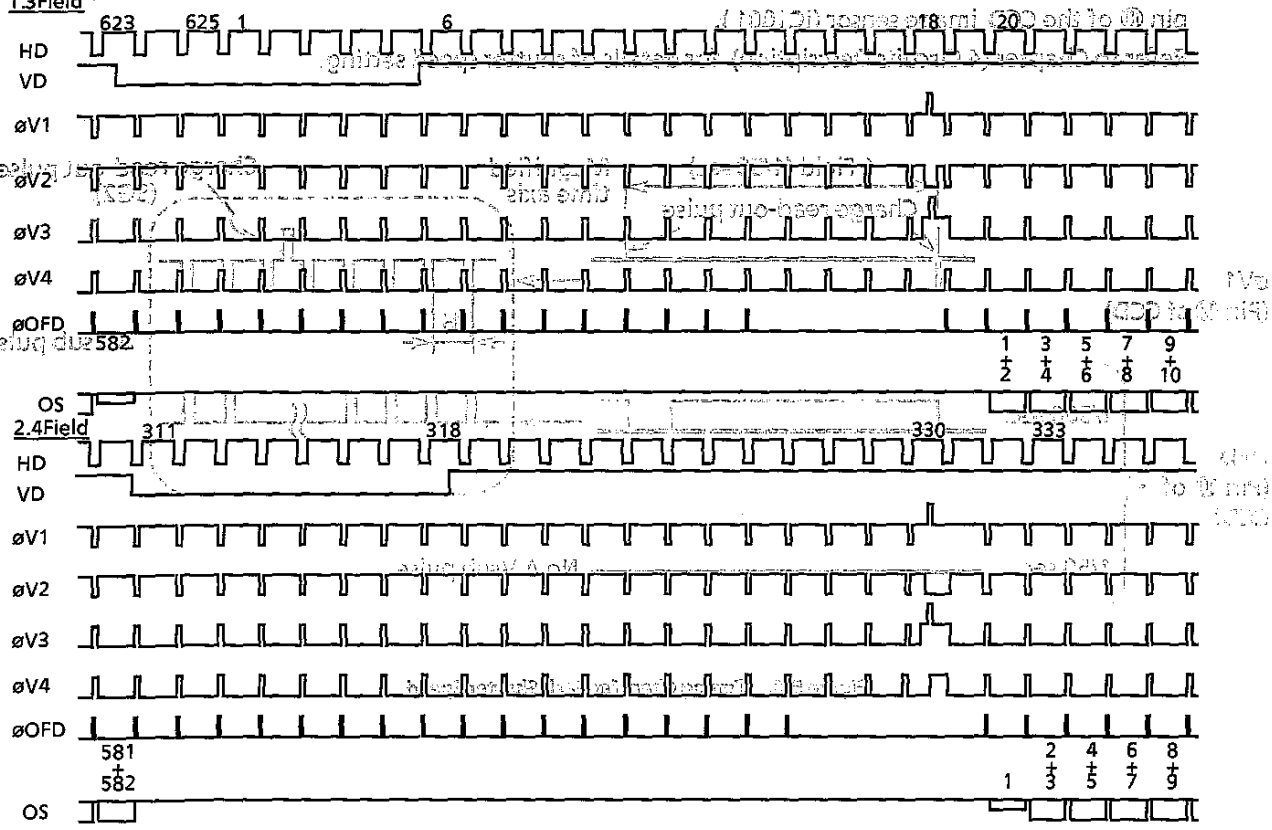


Figure 5-5. Vertical Transfer Timing Chart

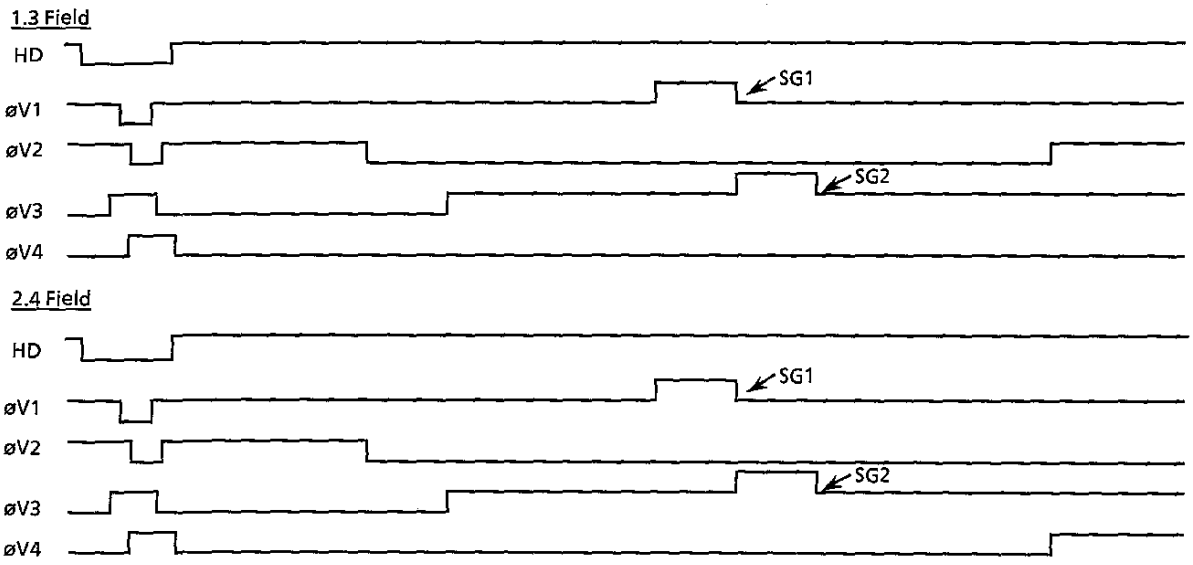


Figure 5-6. Charge Read-Out Timing Chart

① Luminance component (YH signal)

The YH signal component is obtained after the sensor outputs the signal to the CDS (correlated double sampling hold) and then smoothed by the low pass filter.

In Figure 5-9, the YH signal for the n line and n + 1 line in the 1.3 field will be expressed as follows.

$Y_{H(n)} = (G + Ye) + (Mg + Cy)$ ..... n line

$Y_{H(n+1)} = (Mg + Ye) + (G + Cy)$ ..... n + 1 line

The designation of each complementary color filter is shown as :

$Mg = R + B$

$Ye = R + G$

$G = G$

$Cy = G + B$

$$Y_{H(n)} = (G + \overbrace{R + G}^{Ye}) + (\overbrace{R + B}^{Mg} + \overbrace{G + B}^{Cy}) = 2R + 3G + 2B$$

$$Y_{H(n+1)} = (\overbrace{R + B}^{Mg} + \overbrace{R + G}^{Ye}) + (G + \overbrace{G + B}^{Cy}) = 2R + 3G + 2B$$

Therefore, the following expression is obtained.

$Y_H = 2R + 3G + 2B$

The same also applies to the 2.4 field.

In practice, the sensor characteristics and spectral characteristics of the complementary color filter are adjusted to the following theoretical value for broadcasting systems.

$Y = 0.3R + 0.59G + 0.11B$

As shown in Figure 5-10, the sensor output signal (CCD OUT) is supplied to pin ㉟ of HA8144AF. After the CDS (correlated double sampling hold), AGC is outputted from pins ⑨ and ⑩ into pin ㉛ of IC102, and sent out to DSP after A/D conversion.

② Chrominance signal component

The signal outputs (pins ⑨ and ⑩) of IC101 (CDS, AGC) are A/D converted at IC102 to be sent to IC201 for the internal generation of 0H, 1H and 2H.

When the following expressions are available:

$Mg + Ye = C1$

$G + Cy = C2$

$Mg + Cy = C3$

$G + Ye = C4$,

and the r, g and b components of each color filter are defined as follows:

$Mg = r + b$

$Ye = r + g$

$Cy = g + b$

$G = g$,

with the correction values of the color reproducibility:

$Sr = 0.5$

$Sb = 0.5$

$Sg = 1/3$,

then, R, G and B can be separated as shown in the following expressions:

$R = C1 - Sr \times C2 = 2r + 0.5b$

$B = C3 - Sb \times C4 = 2b + 0.5r$

$G = 1/2\{(C2 + C4) - Sg \times (C1 + C3)\} = 5/3G$

The signals C1 and C2 and the signals C3 and C4 are outputted in every 1H, and interpolation signals are produced at CV L.P.F for synchronization.
For the subsequent operations to be processed in a unified system, R, G and B are placed in the 3-point sequential order.
For this, the point sequential signals of C1 C3, and (C2 + C4) and the 3-points sequential signals of C2, C4 and (C1 + C3) are produced to obtain the 3-point sequential signals of R, G and B by subtracting the both after multiplying Sr, Sg and Sb in the color separation block.
Create the following 2-point sequential signals of R-G and B-G from the 3-point sequential signals of R, G and B, and then create signals R-Y and B-Y from the following expression:

R-Y = Gry {(R-G) – Mry (B-G)}
B-Y = Gby {(B-G) – Mby (R-G)}
[Gry, Gby: Color difference gain]
[Mry, Mby: Hue]

6. SIGNAL FLOW

6-1. Summary

This model has reduced a considerable number of parts by processing digitally the signals of the camera section. Described below are the outlines of the camera signal flow. For details of the circuitry operation, refer to the description of each circuit.

- Photo image captured by the lens is converted to a electric signal by CCD image sensor (IC1001) to be inputted into CDS, AGC (IC101).
- CCD OUT signal received by IC101 is processed by IC101 for CDS, GAIN SELECT and AGC, and then sent out as YADIN signal.
- YADIN signal outputted from IC101 is clamped for AD conversion by XCP1 pulse, and then inputted into A/D converter IC (IC102).
- IC102 conducts A/D conversion on YADIN to convert it into 9-bit data for each picture element. Data thus quantized is sent out to DSP (Digital Signal Process: IC201).
- IC201 generates a luminance signal and chrominance signal based on the digital data sent from IC102 and processes them for white balancing, γ correction, knee, and FADE before sending out to D/A converter (IC241) as YDATA and CDATA respectively.
- The luminance signal processed in IC201 goes into 1HDL to become signals 0H, 1H and 2H. Signal 1H drops off the color carrier by going through LPF to become Y signal bus. Each DTL signal of H and V created from signals 0H, 1H and 2H is mixed with the Y signal bus, then applied with CBLK and finally outputted as YDATA together with SYNC after being processed for γ correction, knee, and FADE.
- By processing color signal in IC201, the consecutive signals C1, C2, C3 and C4 are created through interpolation from signals 0H, 1H and 2H sent from 1HDL.
  The signals R, G and B are separated from these signals. For the color signals to be processed in the unified system, the signals R, G and B are placed into the 3-point sequential order. After this, the signals are processed for W/B, γ , knee, and FADE before being converted into R-Y signal and B-Y signal by the color difference matrix circuit. And then they are given subcarrier modulation to be outputted as C DATA.
- D/A converter (IC241) conducts D/A conversion on Y DATA and C DATA respectively to generate analog luminance signal (CAM-Y) and color signal (CAM-C), and they are sent out to the VCR circuit.

7-2. Luminance signal circuits

(1) IC101 (CDS, AGC) and peripheral circuits

CCD OUT signal sent out from the CCD sensor circuit is supplied to pin ⑱ of IC101.
The internal block of IC101 is made up as shown in Figure 7-2.

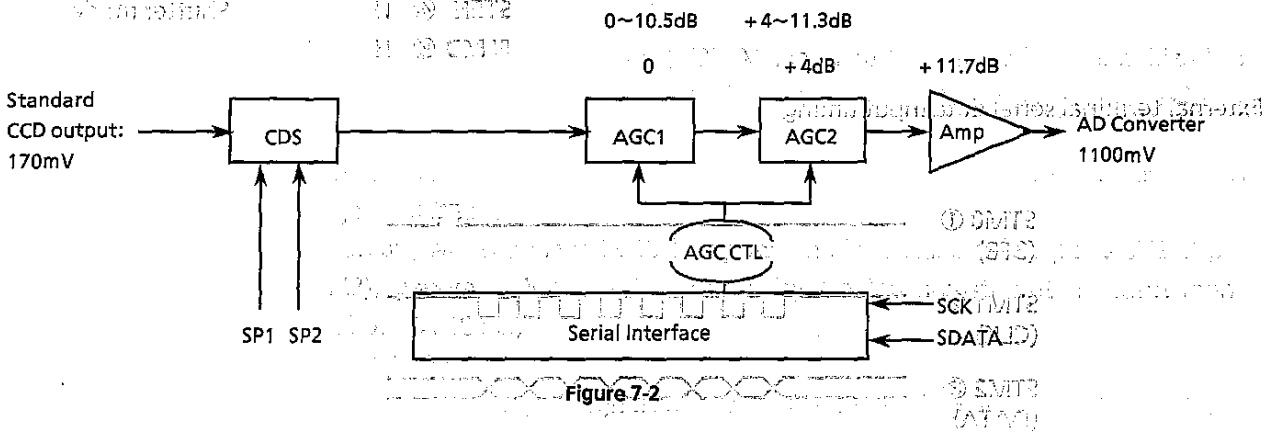


Figure 7-2

1) CDS (correlated double sampling) circuit

CCD image sensor sends out alternatively the noise section (signal for "A" period) and the signal section including noises in it (signal for "B" period). Major noises occurring in the image sensor are low frequency noises and overlaid on signals for output. Accordingly, this may result in the deteriorated S/N.

CDS circuit is made up of a clamp circuit, a sample hold circuit and an inverted amplifier, where low frequency noises are removed by clamping the noise section ("A" period) of image sensor output signals to a fixed voltage, while serial signals are generated by replacing the noise section with the signal section by sample holding the signal section ("B" period) including noises in it. (Refer to Figure 7-3).

- Clamp circuit (CLAMP)

  The noise section ("A" period) of input signal ① is clamped by sample hold 1 (SP1) pulse ② (FCDS, pin ⑫) to a fixed voltage to supply output signal to the sample hold circuit after removing low frequency noises. (Refer to Figure 7-3-(b)-④.)

- Sample hold circuit (SH)

  This is a circuit to sample hold the signal section including noises in it, where the signal section ("B" period) including noises in it is sampled by sample hold 2(SP2) pulse ③ (FS, pin ⑪) and then kept held up to the noise section ("A" period) to generate serial signals by replacing the noise section with the signal section. (Refer to Figure 7-3-(b)-⑤.)

- After being inverted and amplified, the serial signals are supplied to the next gain select circuit.

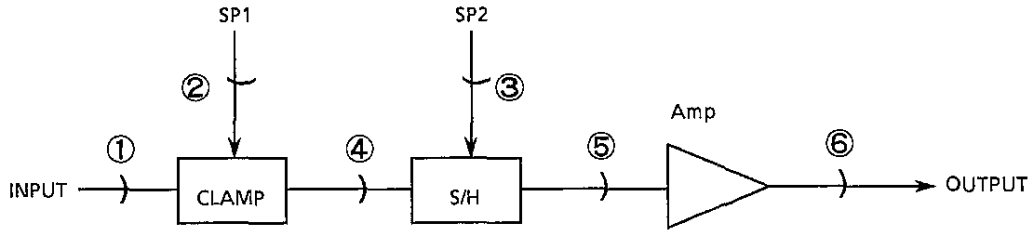


Figure 7-3(a). CDS circuit

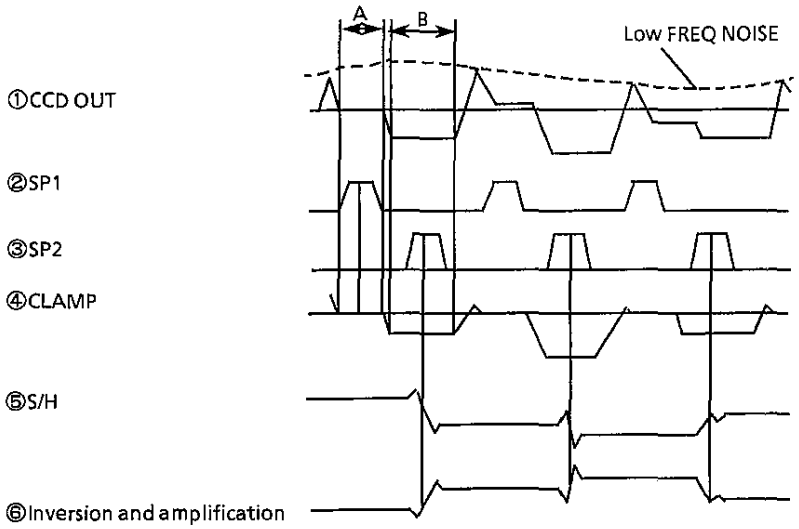


Figure 7-3(b). CDS time chart

2) AGC gain

By serial transfer of 7-bit data with the microcomputer, AGC gain can be set 0 up to 21dB.

In the internal circuit, 21dB variable width is available in AGC1 (preceding part) and AGC2 (succeeding part). For AGC in this model, AGC2 which is set at the standard +4dB raises GAIN gradually up to + 11.3dB, and then AGC1 continues to raise it up to the value from 0dB to 10.5dB.

After AGC, it is amplified to + 11.7dB before being sent out to pins ⑨ and ⑩.

3) A signal outputted from IC101 is clamped at the set up level (Q103) by PDS CTL DC voltage supplied by XCP1 pulse from pin ④ of D/A converter IC503 before being sent to the subsequent A/D converter IC102.

Also, the adjustment of PDS CTL is made by address 75.

(2) IC102 (A/D converter)

This is 9-bit A/D converter where an analog video signal inputted from pin ㉛ is converted into a digital signal before being sent out to the subsequent IC201 (DSP). (D1 to D9)

(3) IC201 (DSP) luminance block

- 9-bit date (D1 to D9) sent from IC102 (A/D converter) goes through YH LPF after 1HDL. At this time, its color carrier is removed to become YH signal.
  This means averaging adjoining picture elements, and can be handled as a luminance signal in either of the following two expressions:
  $YH = (G + Ye) + (Mg + Cy) = (G + R + G) + (R + B + G + B) = 2R + 3G + 2B$

Or

$YH = (Mg + Ye) + (g + Cy) = (R + B + R + G) + (G + G + B) = 2R + 3G + 2B$

For details, refer to the descriptions in "5-5. Color filter."

- Aperture signals are classified into vertical aperture signal and horizontal aperture signal. The vertical aperture signal is made by adding the A/D input signal 0H and the signal 2H with the subtraction of 1H as shown in the following expression:
  $2 \times 1H - (0H + 2H)$
  The vertical aperture signal can set a gain independently. Its setting is made by YDTL VGIN (address 0B).
  The horizontal aperture signal is made by passing through BPF what is obtained by adding signal 0H and signal 2H with 1H added, as shown below:
  $2 \times 1H + (0H + 2H)$
  When the vertical aperture signal and the horizontal aperture signal are mixed, the simultaneous gain setting in both directions is made by YDTL DGIN (address 0C).
  Mixed aperture signals are sliced by YDTL CLPL (address 0D) at the area around its dark section to remove noises before being mixed with YH signal bus.
- Since the data FF of address 0B, 0C or 0D is fixed, be sure not to rewrite it.
- γ correction
  γ correction together with knee correction is displayed in the approximation drawn by 5 broken lines.

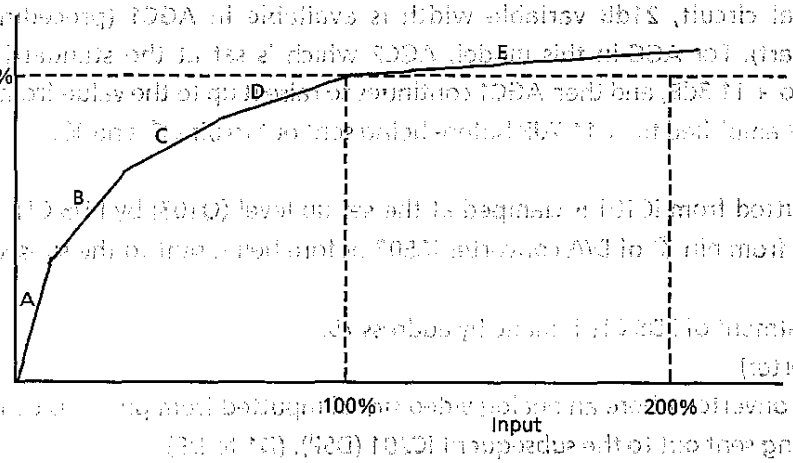


Figure 7-4. γ correction

- γ corrected signal is sent through the fade control circuit via DL for setting up (address 13 data fixed) and SYNC mixing. Then, it is sent out as 8-bit digital luminance signal (YDATA 0 to 7) from pins ⑫ to ⑲ to D/A converter (IC241).

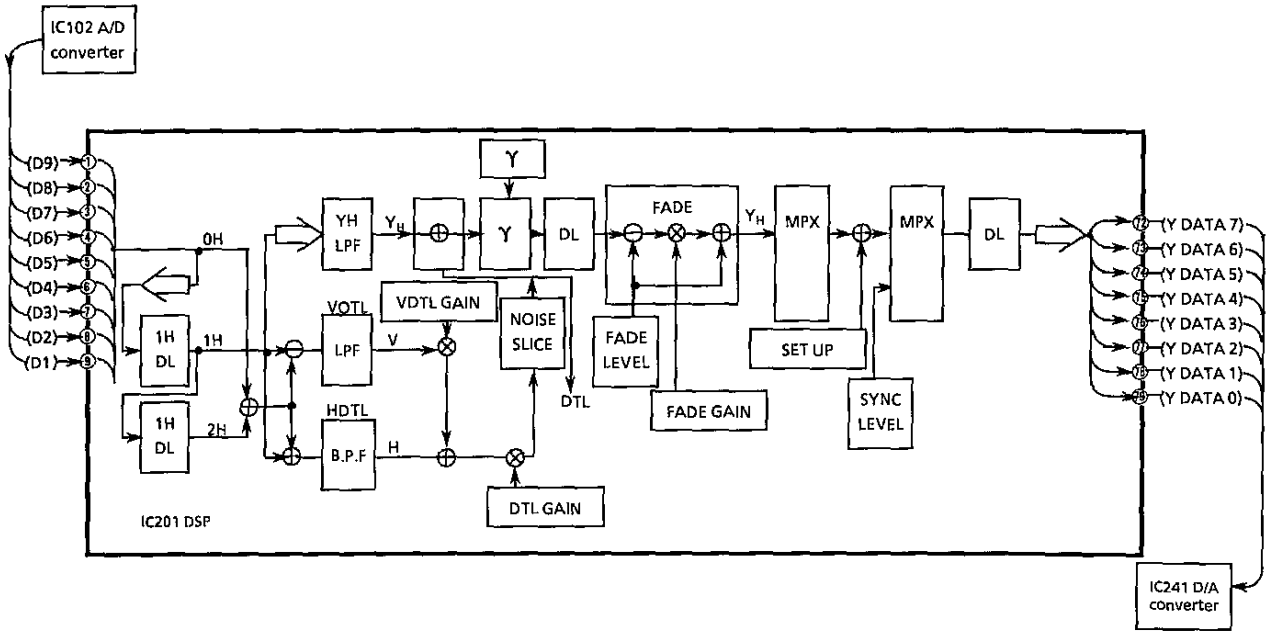


Figure 7-5. DSP luminance signal block diagram

(4) IC241 (D/A converter) and peripheral circuits

A digital luminance signal (YDATA 0 to 7) outputted from DSP is supplied to pins ① to ⑧ of D/A converter. At the same time, it is D/A converted by pin ⑲ of clock signal supplied from DSP and then outputted from pin ㉙ as a luminance signal.

The luminance signal thus outputted goes through peripherals LPF Q241 and Q242 before being sent out to the EE circuit of the VCR section as a camera luminance signal (CAM-Y).

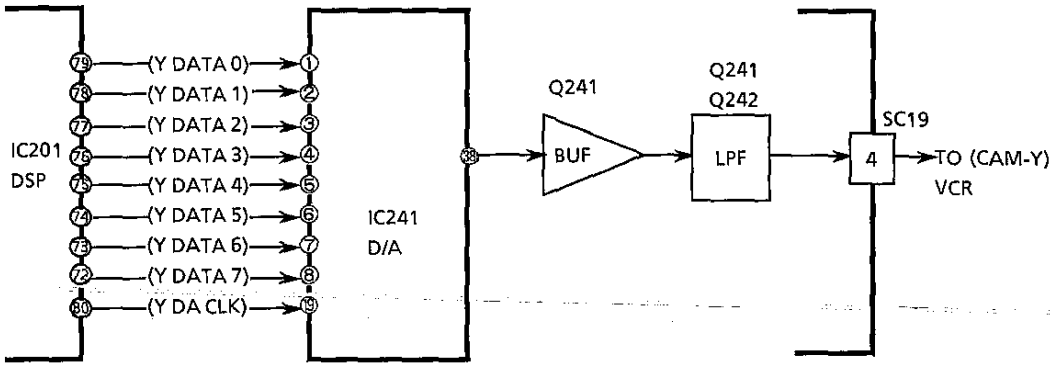


Figure 7-6. Luminance IC241 and peripheral circuits

7-3. Chrominance signal system

Figure 7-7 shows the chrominance signal system block diagram.

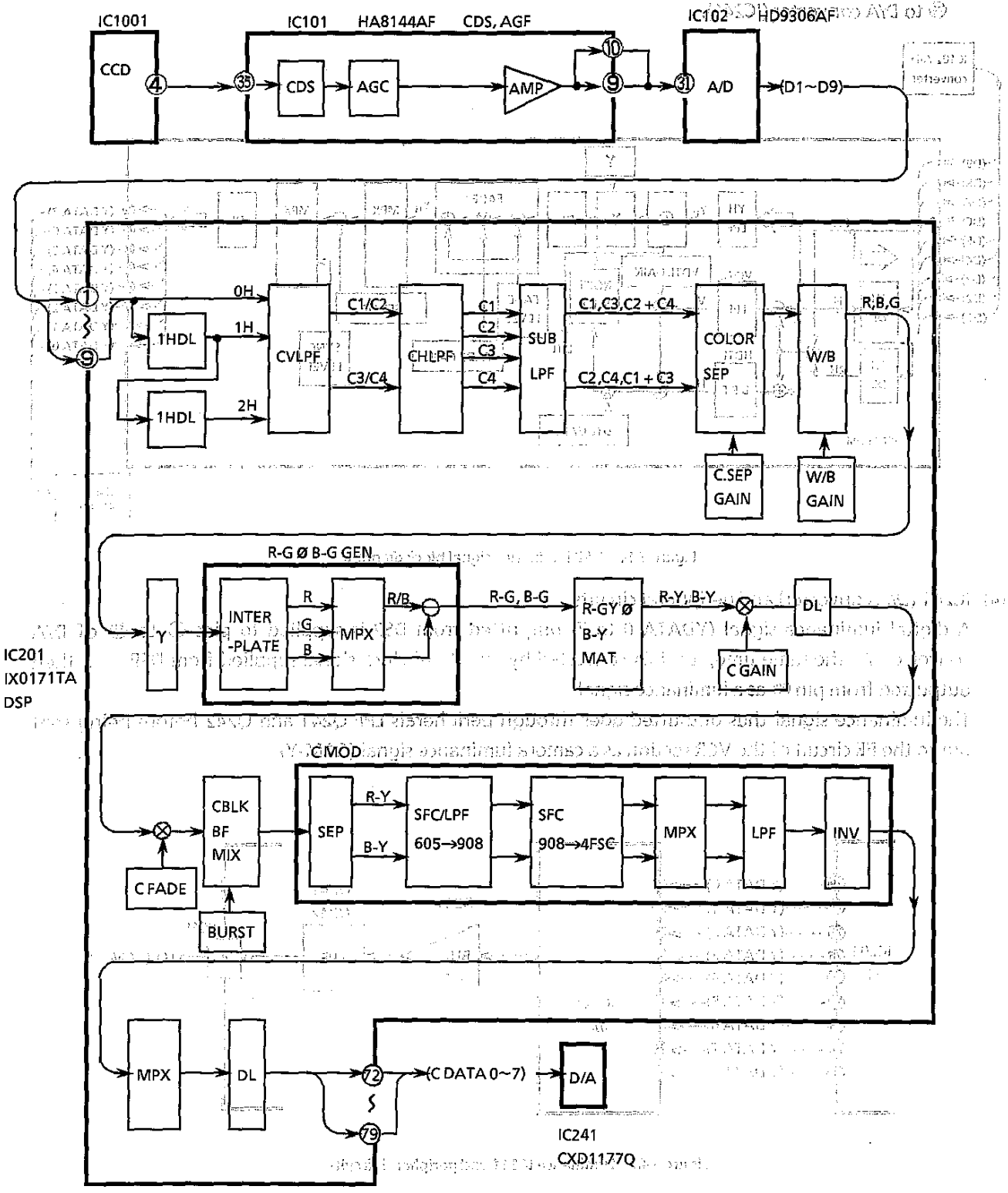


Figure 7-7. Chrominance signal system block diagram

② Horizontal drive (2-phase drive)

Horizontal picture elements are transferred within a single horizontal scan time. The horizontal drive frequency is determined as follows.

$$\text{Horizontal drive frequency} = \frac{1}{\dfrac{\text{Effective horizontal scan time *}}{\text{Electrical effective number of horizontal picture elements}}} = \frac{1}{\dfrac{52.7 \times 10^{-6}\,(\text{sec.})}{503\ (\text{Picture elements})}} \fallingdotseq 9.54\ (\text{MHz})$$

* 63.56 – 10.9 = 52.7 (μsec.)

The frequency is approx. 9.54 MHz, enabling high speed operation.
øH1 and øH2 are square waves of 50% duty with 180° phase difference from each other.
Figure 5-7 shows the horizontal transfer timing chart.

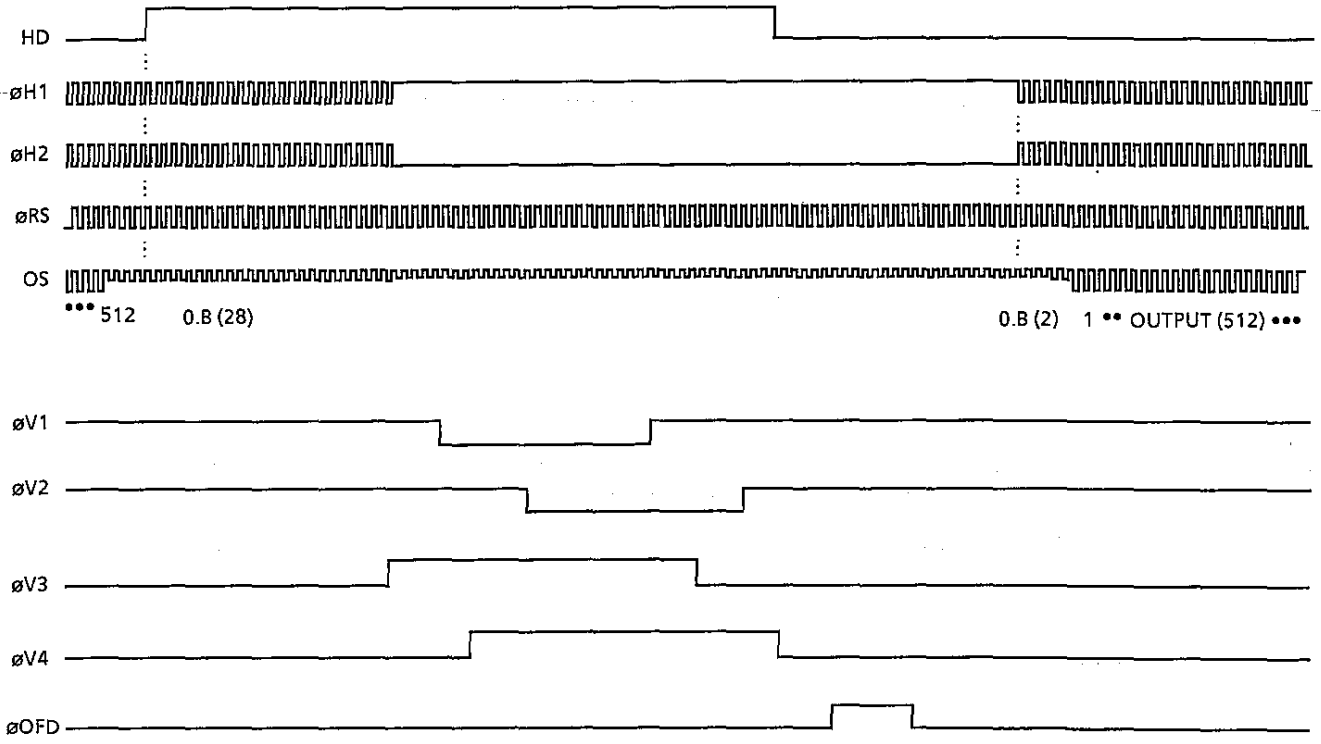


Figure 5-7. Horizontal Transfer Timing Chart

The signals C1 and C2 and the signals C3 and C4 are outputted in every 1H, and the interpolation signals are generated at CV L.P.F for synchronization.
For the subsequent operations to be processed in the unified system, R, G and B are placed in the 3-point sequential order.
For this, the point sequential signals of C1 C3, and (C2 + C4) and the 3-points sequential signals of C2, C4 and (C1 + C3) are generated to obtain the 3-point sequential signals of R, G and B by subtracting the both after multiplying Sr, Sg and Sb in the color separation block.
Create the following 2-point sequential signals of R-G and B-G from the 3-point sequential signals of R, G and B, and then create signals R-Y and B-Y from the following expression:

R-Y = Gry {(R-G) – Mry (B-G)}
B-Y = Gby {(B-G) – Mby (R-G)}
[Gry, Gby: Color difference gain]
[Mry, Mby: Hue]

(1) IC201 DSP (IX0171TA) Color block

- Data sent from A/D converter (IC102) is used as a signal delayed to 0H, 1H and 2H on 1H delay line.
  Signals C1 (= Mg + Ye) and C2 (= G + Cy), and
  signals C3 (= Mg + Cy) and C4 (= G + Ye)
  The above signals are outputted for each 1H, and synchronized by creating an interpolation signal on CVLPF circuit.
- CHLPF is applied with LPF to remove reflection by the subsequent subsampling circuit, while outputting signals C1, C2, C3 and C4 after synchronizing them.
- On subsampling circuit, the following two 3-point sequential signals are produced:
  C1, C3 and (C2 + C4), and
  C2, C4 and (C1 + C3)
- On color separation circuit, R, B and G are separated as the following expressions:
  $R = C1 - Sr \times C2$
  $B = C3 - Sb \times C4$
  $G = 1/2\{(C2 + C4) - Sg \times (C1 + C3)\}$
  However, at this time, color reproducibility can be corrected against the difference of CCD spectral specifications by changing the correction values Sr, Sg, and Sb of color reproducibility.
  R GAIN Adjustment address 50
  B GAIN Adjustment address 51
  When the above two GAIN are provided with G as reference at the time of white projection at 3200°K, white balance is adjusted so that G = R = B (vector center) is resulted by controlling R GAIN and B GAIN.
  Signals R, B and G as 3-point sequential signal carry out γ correction to be sent out to the subsequent step.
- On R-GøR-G GEN circuit, R-G and B-G 2-point sequential signals are created from R, B and G 3-point sequential signals.
- On color difference matrix circuit, when the following expressions are given:
  R-Y = Gry {(R-5) – Mry (B-G)}
  B-Y = Gby {(B-G) – Mby (R-G)}
  then, the color difference matrix R-Y and B-Y are made from 2-point sequential signals R-G and B-G.

Color difference gain correction value Gry	= R-Y Gain	Adjustment address 53
Color difference Gain correction value Gby	= B-Y Gain	Adjustment address 54
Color difference matrix correction value Mry	= R-Y MAT	Adjustment address 56
Color difference matrix correction value Mby	= B-Y MAT	Adjustment address 57

In the above four patterns, signals can be varied. Figure 7-8 shows the changes of the hue at this time.

Shutter speed (in sec.)	Serial data							
	D0	D1	D2	D3	D4	D5	D6	D7
1/500	1	1	0	1	0	1	0	0

External terminals are set as follows:

TVMD ② L ... NTSC mode
PSMD ⑥ L .... Serial mode
STEN ④ H ... Shutter mode
FLMD ⑤ H

External terminal serial data input timing

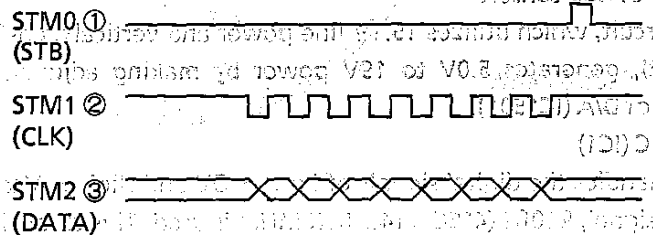


Figure 7-1. Electronic Shutter Control Chart

Synchronized with the rising edge of STM1 signal, STM2 data is shifted to take in 8-bit date. At rising edge of STM0 signal, the data is latched internally.
It is latched again at the falling of horizontal line HD1 signal when the charge read-out pulses (VH1X and VH3X) turn to be active.

(3) Vertical driver IC (IC2)

This IC generates the vertical register drive pulses øV1 to øV4 and the sensor charge draining pulse Vsub used for the high speed shutter based on the pulse timing supplied from the timing IC(IC1).

① øV1 to øV4 reverse and amplify V1X to V4X of the timing IC to make them pulses of Low = −8V and High = 0V. So far as øV1 and øV3 are concerned, VH1X and VH3X pulses (sensor charge read-out pulses) from the timing IC are overlaid on the vertical blanking period. These pulses have Low = 0V and High = 17.5V.

② Vsub regulator sends out a pulse (low = −8V, High = 17.5V) which is obtained after inverting and amplifying the OFD from the timing IC. It is then coupled with OFD power source at C1 and supplied to CCD image sensor.

(4) CCD image sensor (IC1001)

The CCD image sensor is composed of three major sections; a vertical shift register and sensor section, a horizontal shift register section and an output section. For details, refer to the descriptions on "5. CCD OPERATION."

The vertical shift register receives the transfer clock signals øV1 to øV4 (pins ⑫, ⑬, ⑭ and ⑮), while the horizontal shift register receives the transfer clock signals øH1 and øH2 (pins ⑧ and ⑦).

The output section receives +15.1V for the output transistor drain power source (OD, pin ①), and pulses of Low = 2V and High = 6.5V for the reset gate clock (øRS, pin ②).

The output signal is sent from the signal output terminal (OS, pin ④). it is then buffered at Q1001 and supplied to the subsequent IC101 (CDS, AGC:HA8144AF).

7-2. Luminance signal circuits

(1) IC101 (CDS, AGC) and peripheral circuits

CCD OUT signal sent out from the CCD sensor circuit is supplied to pin ㉟ of IC101.

The internal block of IC101 is made up as shown in Figure 7-2.

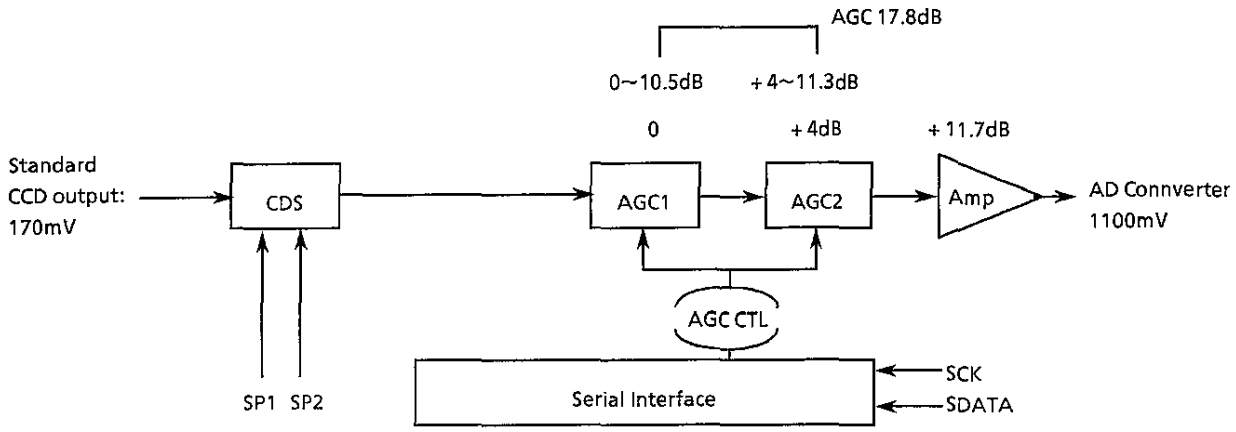


Figure 7-2

1) CDS (correlated double sampling) circuit

CCD image sensor sends out alternatively the noise section (signal for "A" period) and the signal section including noises in it (signal for "B" period). Major noises occurring in the image sensor are low frequency noises and overlaid on signals for output. Accordingly, this may result in the deteriorated S/N.

CDS circuit is made up of a clamp circuit, a sample hold circuit and an inverted amplifier, where low frequency noises are removed by clamping the noise section ("A" period) of image sensor output signals to a fixed voltage, while serial signals are generated by replacing the noise section with the signal section by sample holding the signal section ("B" period) including noises in it. (Refer to Figure 7-3).

- Clamp circuit (CLAMP)
  The noise section ("A" period) of input signal ① is clamped by sample hold 1 (SP1) pulse ② (FCDS, pin ⑫) to a fixed voltage to supply output signal to the sample hold circuit after removing low frequency noises. (Refer to Figure 7-3-(b)-④.)
- Sample hold circuit (SH)
  This is a circuit to sample hold the signal section including noises in it, where the signal section ("B" period) including noises in it is sampled by sample hold 2(SP2) pulse ③ (FS, pin ⑪) and then kept held up to the noise section ("A" period) to generate serial signals by replacing the noise section with the signal section. (Refer to Figure 7-3-(b)-⑤.)
- After being inverted and amplified, the serial signals are supplied to the next gain select circuit.

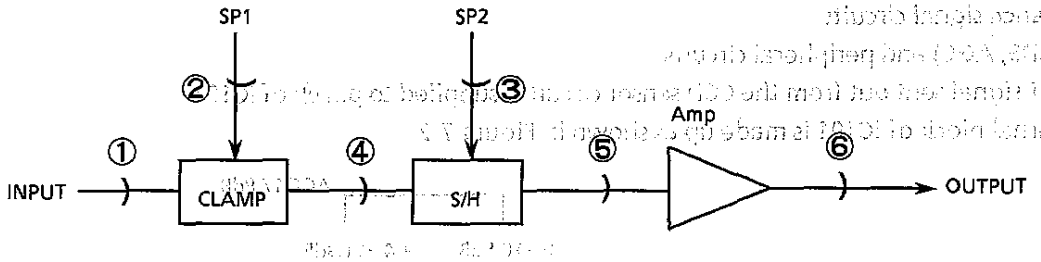


Figure 7-3(a). CDS circuit

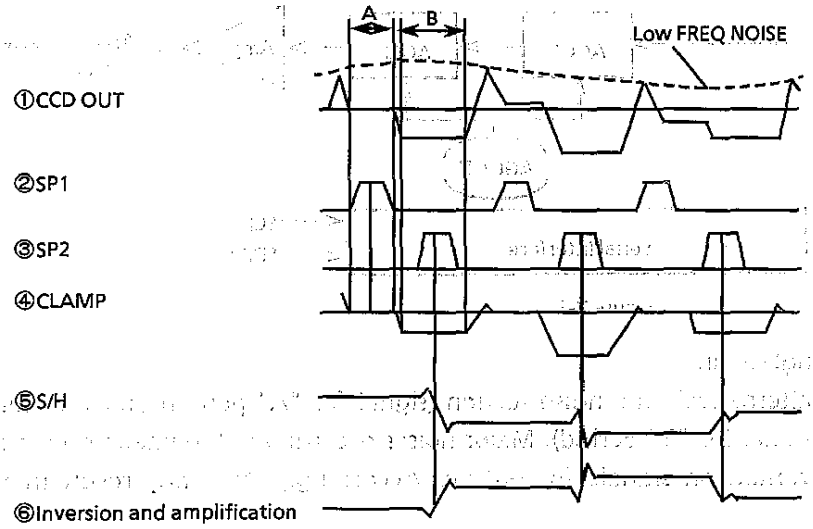


Figure 7-3 (b). CDS time chart

2) AGC gain

By serial transfer of 7-bit data with the microcomputer, AGC gain can be set 0 up to 21dB.

In the internal circuit, 21dB variable width is available in AGC1 (preceding part) and AGC2 (succeeding part). For AGC in this model, AGC2 which is set at the standard +4dB raises GAIN gradually up to +11.3dB, and then AGC1 continues to raise it up to the value from 0dB to 10.5dB.

After AGC, it is amplified to +11.7dB before being sent out to pins ⑨ and ⑩.

4) A signal outputted from IC101 is clamped at the set up level (Q103) by PDS CTL DC voltage supplied by XCP1 pulse from pin ④ of D/A converter IC503 before being sent to the subsequent A/D converter IC102.

Also, the adjustment of PDS CTL is made by address 75.

(2) IC102 (A/D converter)

This is 9-bit A/D converter where an analog video signal inputted from pin ㉛ is converted into a digital signal before being sent out to the subsequent IC201 (DSP). (D1 to D9)

(3) IC201 (DSP) luminance block

- 9-bit date (D1 to D9) sent from IC102 (A/D converter) goes through YH LPF after 1HDL. At this time, its color carrier is removed to become YH signal.
  This means averaging adjoining picture elements, and can be handled as a luminance signal in either of the following two expressions:
  YH = (CY + Mg) + (Ye + G) = (G + B + R + B) + (R + G + G) = 2R + 3G + 2B
  Or
  YH = (Cy + G) + (Ye + Mg) = (G + B + G) + (R + G + R + B) = 2R + 3G + 2B
  For details, refer to the descriptions in "5-5. Color filter."
- Aperture signals are classified into vertical aperture signal and horizontal aperture signal. The vertical aperture signal is made by adding the A/D input signal OH and the signal 2H with the subtraction of 1H as shown in the following expression:
  2 x 1H – (0H + 2H)
  The vertical aperture signal can set a gain independently. Its setting is made by YDTL VGIN (address 0B).
  The horizontal aperture signal is made by passing through BPF what is obtained by adding signal 0H and signal 2H with 1H added, as shown below:
  2 x 1H + (0H + 2H)
  When the vertical aperture signal and the horizontal aperture signal are mixed, the simultaneous gain setting in both directions is made by YDTL DGIN (address 0C).
  Mixed aperture signals are sliced by YDTL CLPL (address 0D) at the area around its dark section to remove noises before being mixed with YH signal bus.
- Since the data FF of address 0B, 0C or 0D is fixed, be sure not to rewrite it.
- γ correction
  γ correction together with knee correction is displayed in the approximation drawn by 5 broken lines.

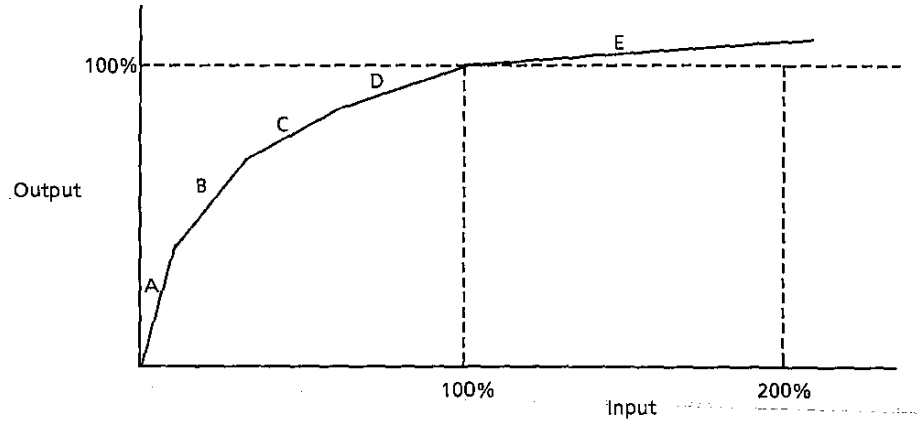


Figure 7-4. γ correction

- γ-corrected signal is sent through the fade control circuit via DL for setting up (address 13 data fixed) and SYNC mixing. Then, it is sent out as 8-bit digital luminance signal (YDATA 0 to 7) from pins ㉒ to ㉙ to D/A converter (IC241).

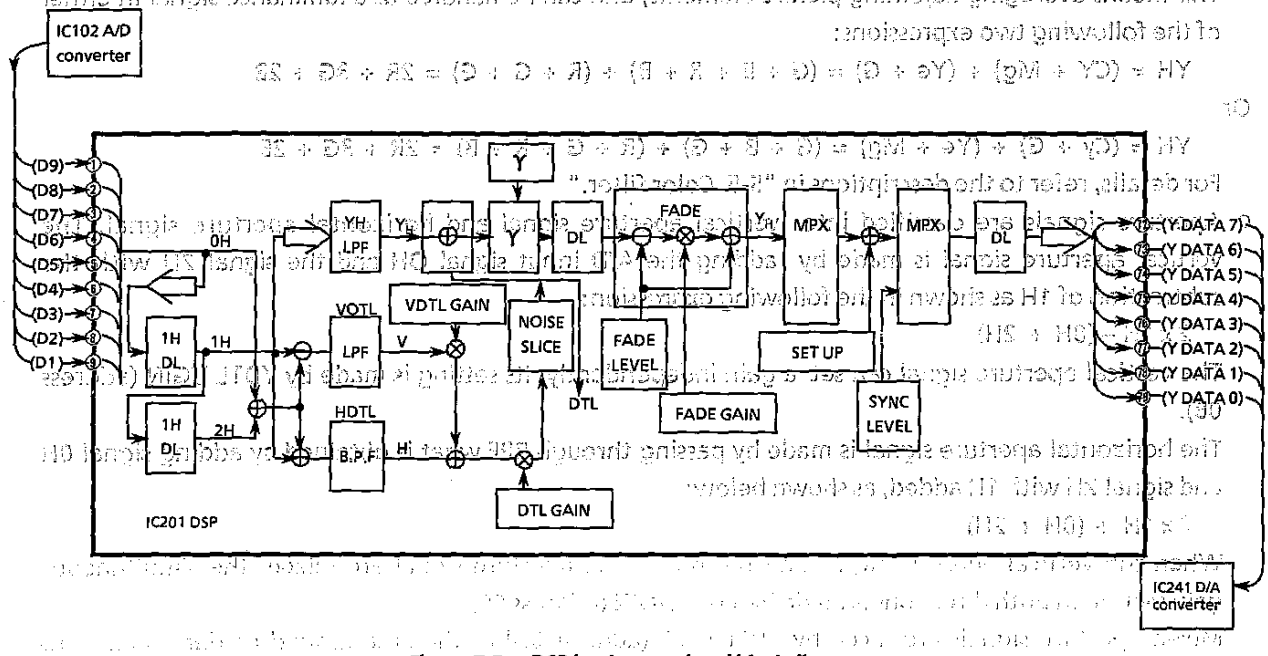


Figure 7-5. DSP luminance signal block diagram

(4) IC241 (D/A converter) and peripheral circuits

A digital luminance signal (YDATA 0 to 7) outputted from DSP is supplied to pins ① to ⑧ of D/A converter. At the same time, it is D/A converted by pin ⑨ of clock signal supplied from DSP and then outputted from pin ㉙ as a luminance signal.

The luminance signal thus outputted goes through peripherals LPF Q201 and Q202 before being sent out to the EE circuit of the VCR section as a camera luminance signal (CAM-Y).

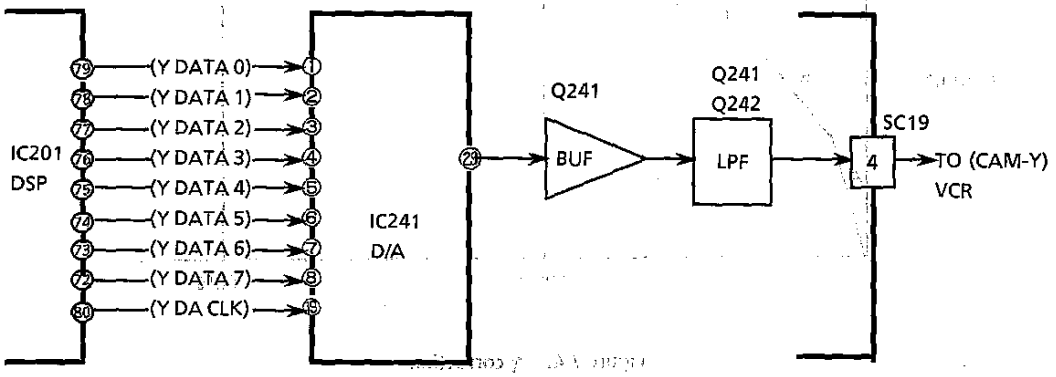


Figure 7-6. Luminance IC241 and peripheral circuits

7-3. Chrominance signal system

Figure 7-7 shows the chrominance signal system block diagram.

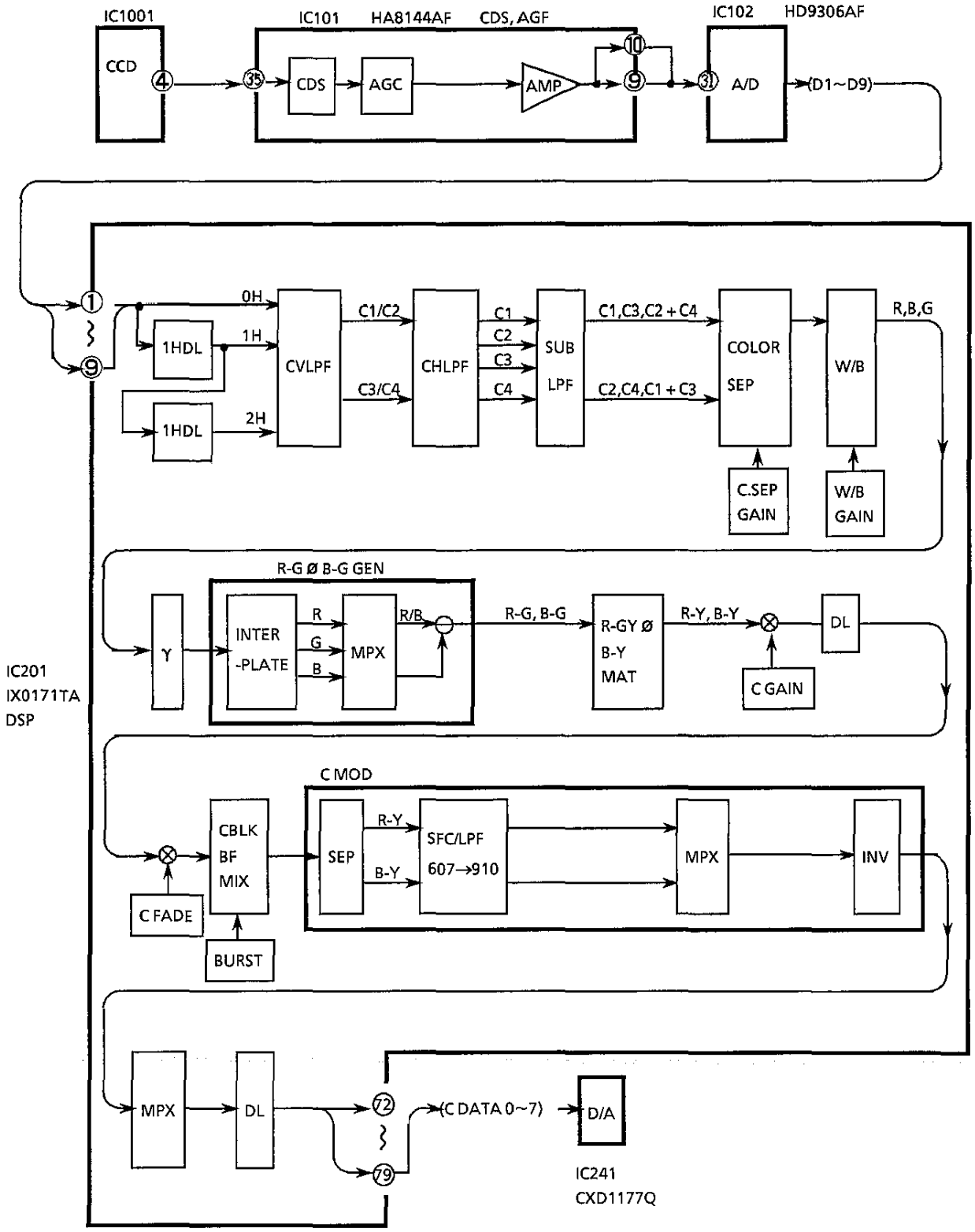


Figure 7-7. Chrominance signal system block diagram

(1) IC201 DSP (IX0171TA) Color block

- Data sent from A/D converter (IC102) is used as a signal delayed to 0H, 1H and 2H on 1H delay line.
  Signals C1 (= Ye + Mg) and C2 (= Cy + G), and
  signals C3 (= Cy + Mg) and C4 (= Ye + G)
  The above signals are outputted for each 1H, and synchronized by creating an interpolation signal on CVLPF circuit.
- CHLPF is applied with LPF to remove reflection by the subsequent subsampling circuit, while outputting signals C1, C2, C3 and C4 after synchronizing them.
- On subsampling circuit, the following two 3-point sequential signals are produced:
  C1, C3 and (C2 + C4), and
  C2, C4 and (C1 + C3)
- On color separation circuit, R, B and G are separated as the following expressions:
  $R = C1 - Sr \times C2$
  $B = C3 - Sb \times C4$
  $G = 1/2\{(C2 + C4) - Sg \times (C1 + C3)\}$
  However, at this time, color reproducibility can be corrected against the difference of CCD spectral specifications by changing the correction values Sr, Sg, and Sb of color reproducibility.
  R GAIN Adjustment address 50
  B GAIN Adjustment address 51
  When the above two GAIN are provided with G as reference at the time of white projection at 3200°K, white balance is adjusted so that G = R = B (vector center) is resulted by controlling R GAIN and B GAIN.
  Signals R, B and G as 3-point sequential signal carry out γ correction to be sent out to the subsequent step.
- On R-GøR-G GEN circuit, R-G and B-G 2-point sequential signals are created from R, B and G 3-point sequential signals.
- On color difference matrix circuit, when the following expressions are given:
  R-Y = Gry {(R-5) – Mry (B-G)}
  B-Y = Gby {(B-G) – Mby (R-G)}
  then, the color difference matrix R-Y and B-Y are made from 2-point sequential signals R-G and B-G.
  Color difference gain correction value Gry = R-Y Gain Adjustment address 53
  Color difference Gain correction value Gby = B-Y Gain Adjustment address 54
  Color difference matrix correction value Mry = R-Y MAT Adjustment address 56
  Color difference matrix correction value Mby = B-Y MAT Adjustment address 57
  In the above four patterns, signals can be varied. Figure 7-8 shows the changes of the hue at this time.

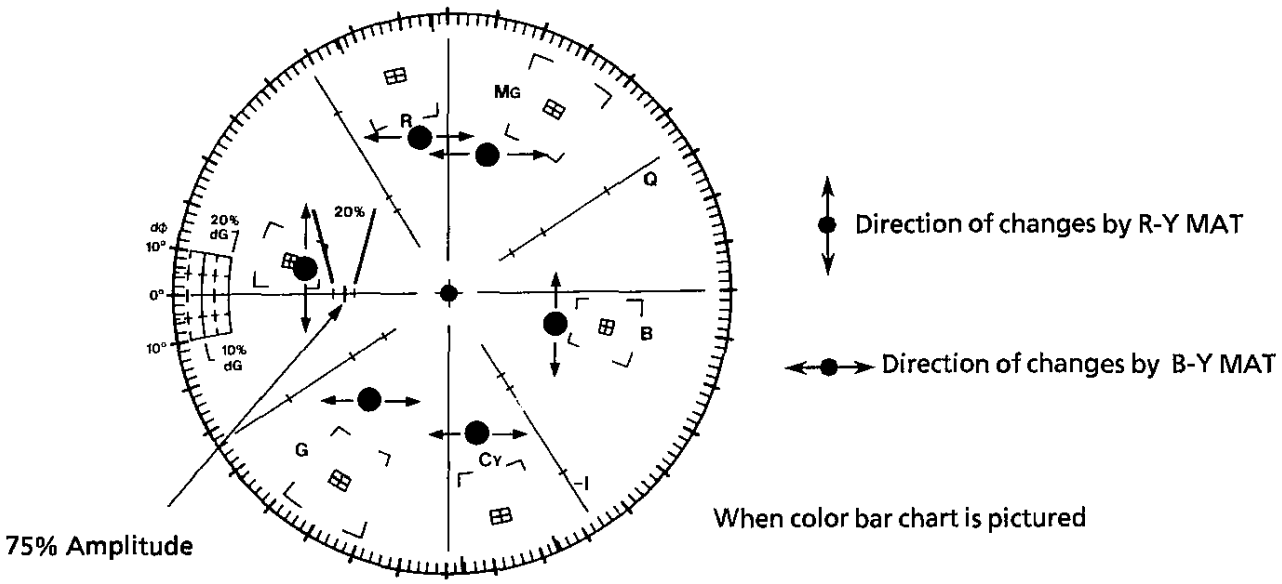


Figure 7-8. Hue Control

Each control of R GAIN, B GAIN, R-Y GAIN, B-Y GAIN, R-Y GAIN, R-T MAT and B-Y MAT is made by sending address and data from the microcomputer through the interface with camera μ-CON (IC501) at pin ⑮ (DATA), pin⑫ (DSPST) and pin ⑭ (CLK).

- The color difference matrix signals R-Y and B-Y carry out color modulation after mixing of burst with blanking section. Then, they are supplied to D/A converter (IC241) from pins ⑩ to ⑰ as 8-bit digital macro signals (CDATA 0 to7).

(2) IC241 D/A converter (CXD1177Q) and peripheral circuits

Digital chroma signals (CDATA 0 to 7) outputted from DSP (IC201) are supplied to pins ⑨ to ⑯ of D/A converter IC, while clock signals (CDACLK) outputted from DSP are D/A converted by pin ⑳ before being sent out from pin ㉗ as analog chroma signals.

The chroma signals thus outputted go through Q243 low pass filter and Q244 peripheral band pass filter, and then they are sent out as camera chroma signals (CAM-C) to the EE circuit of VCR section through ⑲pin FPC connected to SC19.

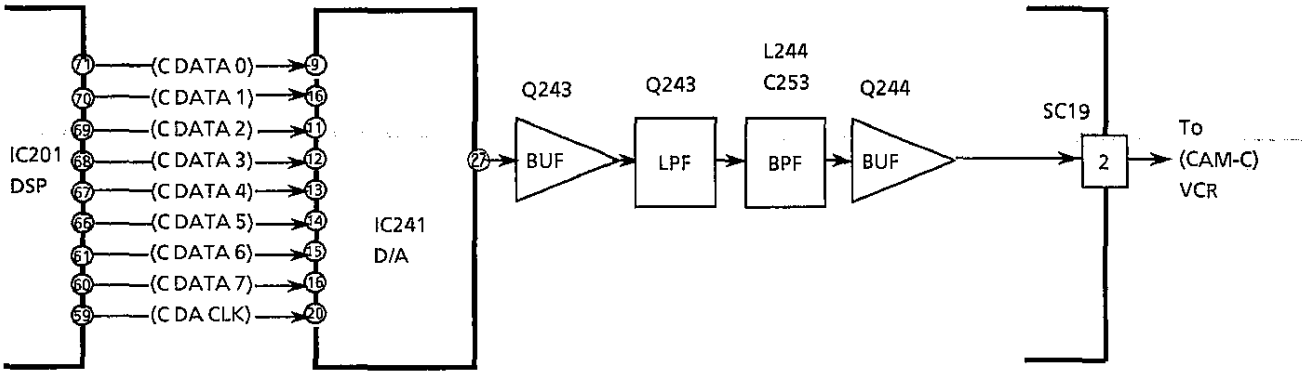


Figure 7-9. Chroma system IC241 peripheral circuit.

8. AUTO WHITE BALANCE

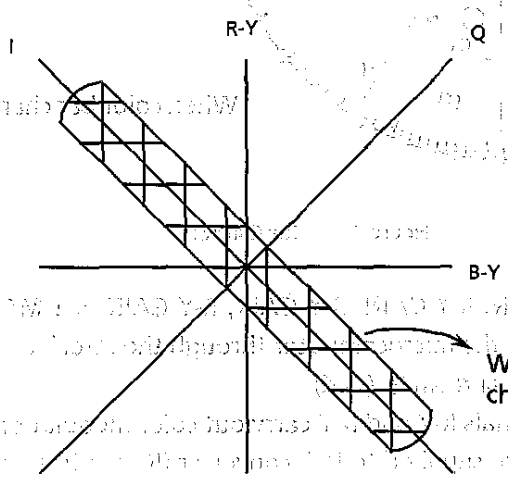
8-1. Method

Digital signal processing method

IQ conversion white component extraction method

8-2. Operating principle

Since the direction of the shift in white balance caused by the change of a color temperature is roughly in line with the I axis, R-Y and B-Y signals are converted into I and Q signals before being taken into the microcomputer. The microcomputer then determines light source and photographing conditions based on the level of I and Q signals and luminance information to make a necessary adjustment for the optimum white balance.



※I and Q signals are signal names used for NTSC method. However, since the design concept is shared by NTSC and PAL, the name of I and Q signals is used for convenience.

8-3. White balance mode

There are two type of modes available:

- Auto
- Lock

※ Even while in auto mode, the system gets locked when one of the following conditions is met.

① When white balance occurs.

② When the light is shaded.

③ When a sufficient correction cannot obtained even when correction is made up to the clip value.

④ While in zooming up

8-4. White balance adjustment

IN DOOR 2 ch. (Adjustment of a convergent point while in "Auto" operation with I and Q signal levels stored in memory)

OUT DOOR 2 ch. (Adjustment of the clip point of a high color temperature)

As shown above, the total of 4 channels are adjusted.

8-5. Control range

Approxi. 3000k to 7000k

The correction of I axis is so decided that the range above is covered, while the Q axis correction is restricted to the range where the difference from I axis at the time of the I axis correction can be corrected.

8-6. Operation

① IQ conversion (IC506 digital auto IC)

Based on R-Y and B-Y data from DSP, get the levels of the I and Q signals from the following expressions.

$I = (R-Y) + a \times (B-Y)$

$Q = (B-Y) + b \times (R-Y)$

② Data compression, or gate (IC506 digital auto IC)

Compare I and Q data thus obtained from the above with the comparison data from the microcomputer, and compress or gate the data whose point is larger between I and Q level. White color is extracted in this manner to detect the shift.

③ Data integration (IC506 digital auto IC)

Date IQ-converted are compressed or gated and then integrated in digital auto IC.

④ Data input (IC501 camera microcomputer, IC506 digital auto IC)

The camera microcomputer supplies address to digital auto IC and reads sequentially I and Q data for processing.

⑤ Control output (IC501 camera microcomputer, IC201 digital signal process)

Output data from the camera microcomputer are sent out as serial data to digital signal process IC to control white balance.

Control is made so that I and Q data to be inputted into the camera microcomputer get become I and Q levels stored in memory while in IN DOOR adjustment.

8-7. Operating speed

The operating speeds of A/W are shown below:

Operating speed	Quick ←——————→	Slow
Shift amount	Large	Small
Picture angle	Wide	Tele
OK→NG	Long elapsed time	Short elapsed time

However, when power is turned on, the system employs high speed operation to fall back in about 1 second. When there occurs white balance once, it will not restart for a fix period of time (about 4 seconds).

8-8. Presumption of light source (Fuzzy logic)

Light source is presumed based on luminance information and current correction data.

(When in one axis correction mode)

Small R GAIN	→ Halogen or cool white fluorescent light
Dim and large R GAIN	→ 3-wavelength daylight, or daylight fluorescent light
Bright and large R GAINS	→ Sun beam

(When in Two axes correction mode)

Bright and small R GAIN	→ Halogen
Dim	→ Fluorescent light, at dusk
Bright and large R GAIN	→ Sun beam

The fuzzy rule varies according to CCD characteristics. Correction should be made based on these assumptions so that the optimum white balance is obtained at all times.

9. AUTO FOCUS

9-1. Basic behavior

This unit employs a video signal type auto focus. Its basic operation is to make focusing by driving the lens according to the size of the high-frequency component included in the video signal obtained through the CCD sensor. The principle of operation is as follows. When the focus lens is moved forward and backward, if the image-formation position is shown by x-axis and the video signal high frequency component size by y-axis, the high frequency component size follows a hill-like shape which has a peak indicating the focusing point. Focusing is made by detecting the direction (inclination) of this hill, going up the hill and reaching the peak.

(1) Outline of auto focus operation

The digital signal (AFY0~9) from the digital signal processing section is subjected to digital filter to be divided into high-frequency data and low-frequency data in the digital gate array (IC506), which are integrated after experiencing the view angle gate (area for obtaining the focus detection signal) processing. Those are the following data, which are sent to the camera microprocessor as detection signal.

a) Center view angle high-frequency data
b) High-frequency data (wide-angle or longitudinal)
c) Low-frequency data (wide-angle or longitudinal)

For the high-frequency data and low-frequency, the camera microprocessor changes the setting of IC506 so that the wide-angle or longitudinal area is provided according to the focus information (condition of focus operation, condition of zoom operation, focus detection signal amount, etc).

Based on the change of the focus detection signal, the camera microprocessor sends the phase pulse (DA1, DA2) and power control signal (FC) for focus motor driving to the motor driver IC (IC552). The motor driver IC drives the motor according to the phase pulse, and the focus motor moves the focus lens forward and backward.

The condenser connected to pins (3) and (6) of the driver IC is used to make the motor driving waveform trapezoidal for reducing the noise generated at motor driving.

The detection data increases and decreased as the focus lens moves forward and backward, and the camera microprocessor determines the peak (focusing point) of the detection data to make focusing.

(2) Outline of focus operation by zoom

Because of the rear lens focus method, in order to keep the focal distance constant, it is necessary to change the focus lens according to the change of the zoom lens.

It is called zoom tracking correction. The relation between the zoom lens position and focus lens position is as shown in Fig.9-3.

As a result, high accuracy tracking correction is realized.

In zoom tracking correction, as shown in Fig.9-4, two tracking curves for 1 m distance and ∞ distance are stored as data in the microprocessor. The focus lens is controlled so that, when the zoom is moved from the reference position (the present focal distance), the ratio of the step distance between 1m and ∞ to the step distance between reference focus position and ∞ is the same at the reference zoom position.

While always performing addition and subtraction of the number of the driving pulses sent to the stepping motor, the camera microprocessor monitors the present focus lens position.

In order to set the reference position of the focus lens, the edge of the shielding plate moving together with the focus lens is detected by the photo-interrupter and the resulting voltage change is used by pin (32) (PHIR) of the camera microprocessor.

9-6. Camera microcomputer operation (Auto focus program)

1) Operation when the power is on

The camera microcomputer runs the stepping motor while counting the number of the driving pulses, and searches the focus lens position at which the signal from the photo interrupter varies.

After storing in the memory the position at which the signal varies as the reference position, it returns the focus lens to its original position.

2) Stepping motor control

By adding and subtracting continuously the number of the driving pulses sent out to the stepping motor, the camera microcomputer keeps monitoring the current focus lens position against the reference position.

3) Zoom motor control

The zoom motor is controlled in the same way as in the above items 1) and 2).

4) Basic focusing operation

The camera microcomputer compares the integrated data sent from the digital auto LSI in every 3-V cycle in order to obtain the focal point.

It calculates the focal point direction from the change in the data amount before and after the focus lens movement.

When the focal point is found two times, the microcomputer compares the peak position for the first and second times. If the result of the comparison is judged to be the true peak position, it confirms the focal point before locking.

By repeating the above operations, the focus lens is moved to the point at which the maximum integrated date is obtained.

5) Integrated data usage

The high-band integrated signal and the low-band integrated signal are inputted from the digital auto LSI into the camera microcomputer, and the microcomputer makes selections between these signals while in the focusing operation.

Since the high-band data is obtained only near the focal point, the camera microcomputer moves the focus lens in the direction where the low-band data increases when the lens is considerably out of focus. When the high-band data is found, it searches the focus lens position at which the high-band data reaches maximum.

6) Gate selection (Focus area change)

By changing the AF picture angle in the digital auto SLI, the camera microcomputer makes selection in the order of the wide angle, the longitudinal, the centering and the narrow angle.

When no integrated data is obtained even by moving the focus lens through its entire range, or when the peak of the integrated data is quite low, the gate is enlarged.

7) Operation by zoom position detection

The camera microcomputer always monitors the zoom lens position to control the focusing.

The effective range of the focus lens varies in accordance with the change in the position of the zoom lens. The amount of the focus lens travel to change the focal length decreases in the wide-angle direction and increases in the telescope direction.

Also, the depth of "field" (the range of the focal length at which the image is focused) varies with the changes in the zoom lens position.

The microcomputer controls the focus lens moving range and moving speed so that the optimum focusing operation is obtained against the above mentioned optical variations caused the changes in zooming operation.

When the focus is manually adjusted, the following operation is performed because of the relationship between the zoom lens position and the focal length:
That is, in order to maintain the focal length manually set by the user, the zoom tracking correction is carried out by moving the focus lens in accordance with the zoom lens movement when the zoom lens is operated.

8) Operation by detection through the hall sensor
The iris is always monitored for proper focus adjustment.
The depth of field of the lens varies according to the opening amount of the iris. When the field is deep with the iris closed, the change in the integrated data gets smaller against the focus lens travel, and on the contrary, when the field is shallow with the iris open, the integrated data variation gets larger against the focus lens travel.
From this relationship, the microcomputer controls the amount of the focus lens travel in 3-V cycle according to the opening amount of the iris.

9) Operation by detecting AGC state
When the iris gets open due to the object being dark and the AGC circuit gain in the signal processing circuit increases, noises in the AF-Y signal also increase. Noises that correspond with the band in the digital filter are made into integrated data as they are.
The camera microcomputer shifts the absolute values of the integrated data according to the control voltage of the AGC circuit.

10) Operation by zoom control
The camera microcomputer controls the zoom motor by adding or subtracting the number of driving pulses. While the zoom lens is being moved in the wide-angle direction, the focus lens is also moved in accordance with the zoom tracking correction from the focus lens position just before the zoom lens operation started.

(5) BL5V circuit

This circuit feeds the control signal "BL-C" outputted from pin (4) of D/A converter of IC807 to pin (4) of IC901 to perform voltage-pulse width conversion through the PWM comparator. The input control signal further drives Q961 (FP101). Then, it is smoothed through L961 (22 µH) and C966 (3.3 µF) and outputted as BL5V. 5V is outputted at the time when the power source is turned on, but it comes down to 2.8V after approximately 90 seconds.

(6) Motor driving circuit

Control signals "DRUM ERR" and "CAP ERR" outputted from the ATF circuits of the drum motor and capstan motor are inputted to error amplifiers 3ch and 4ch (IC900) and subjected to voltage-pulse width conversion in the PWM comparator, after which they drive Q902 (FP101) and Q903 (FP101) respectively. Then they are outputted as DRUM-VS and CAP-VS after experiencing LC smoothing. At normal REC PB, DRUM-VS is about 2V and CAP-VS is about 1.8V.

14. SYSTEM CONTROL CIRCUIT (RH-IX0164TAZZ)

14-1. Outline

The system control circuit of this unit is controlled by IC701. IC701 contains software which controls the mechanism of the unit, sensors, on/off operation of the power source, camera microprocessor, communication with the tuner microprocesser, key input, character display, etc. This microprocessor makes it possible to correspond to the specifications of each destination (specifications of some destinations are excluded) or OEM. Switching can be made by means of EEPROM.

Block Diagram of System

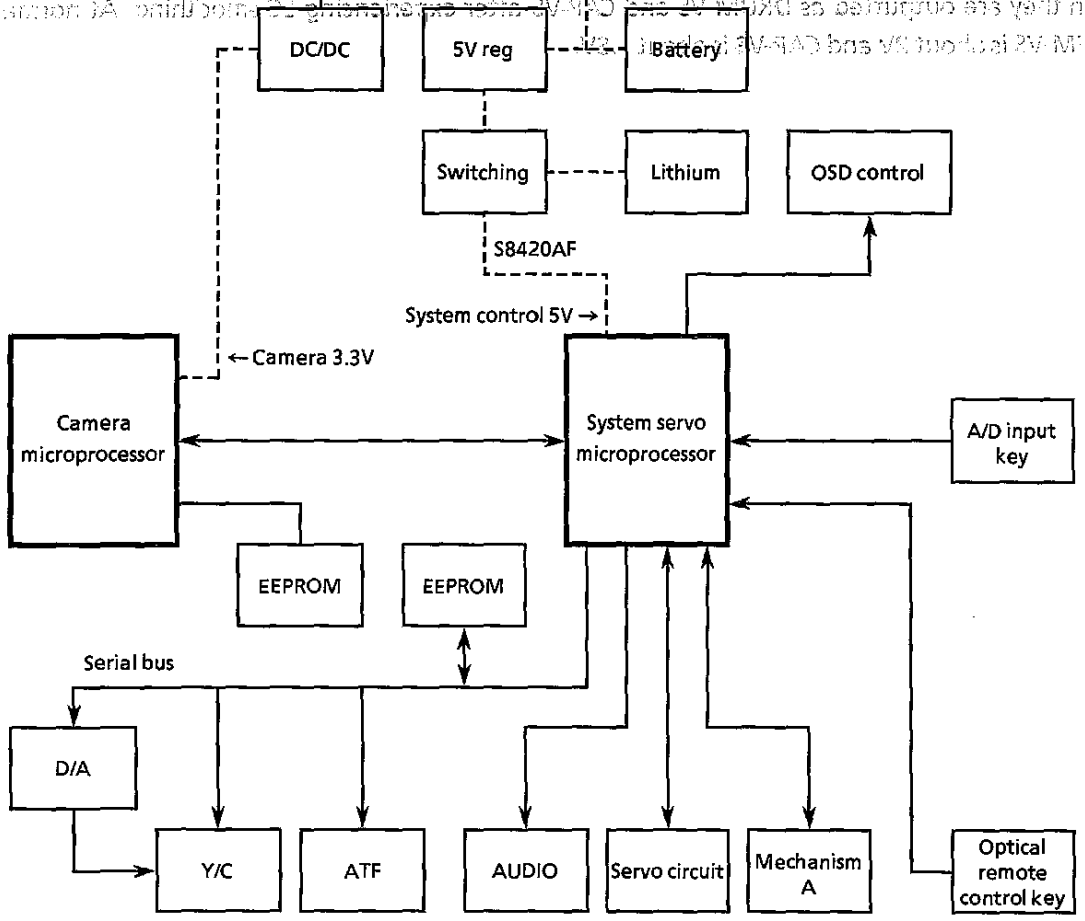


Table 14-1. Arrangement of Terminals (100VQFP 0.50 mm pitch)

* Status of port when microprocessor is reset (Z.....high impedance)

No.	Pin name	IO	Form	※	Pin function name	Function
1	PB3/PP011/A3	O	cmos	Z	H-SW-P	Video head switching pulse output terminal.
2	PB2/PP010/A2	O	cmos	Z	JOG	"H" output terminal for variable speed playback.
3	PB1/PP09/A1	O	cmos	Z	JOG VD H	Pseudo VD output terminal to be inserted at variable speed playback.
4	PB0/PP08/A0	O	cmos	Z	WH	Control signal for LCD noiseless write. "H": Write.
5	PC7/RT07/D7	O	cmos	Z	REF30Hz	Servo reference signal 30 Hz.
6	PC6/RT06/D6	O	cmos	Z	P-CON-H	Main DC-DC converter control signal. "H" when power is turned on.
7	PC5/RT05/D5	I	Hi-z	Z	ME/$\overline{MP}$	Tape type identification. "H" when ME tape is used.
8	PC4/RT04/D4	I	Hi-z	Z	TURN SW	Self record shooting mode detection switch. "L" at the time of self record shooting.
9	PC3/RT03/D3	I	Hi-z	Z	PROTECT SW	Error erase prevention switch. "L" at normal operation.
10	PC2/PP02/D2	I	Hi-z	Z	SW-C	Mechanism position detection switch. "L" when switch is turned on.
11	PC1/PP01/D1	I	Hi-z	Z	SW-B	
12	PC0/PP00/D0	I	Hi-z	Z	SW-A	
13	PJ7	I	Hi-z	Z	CAMERA SW	CAMERA SW (Standby reset)
14	PJ6	I	Hi-z	Z	EJECT SW	EJECT SW (Standby reset)
15	PJ5	I	Hi-z	Z	VCR SW	VCR SW (Standby reset)
16	PJ4	I	Hi-z	Z	CASCON SW	Low when cassette controller switch input is down. (Standby reset)
17	PJ3	I	Hi-z	Z	VCR ADJ	VCR automatic adjustment. "L" allows to shift to automatic adjustment mode. (Standby reset)
18	PJ2	I	Hi-z	Z	CAM ADJ	Camera automatic adjustment. "L" allows to shift to automatic adjustment mode. (Standby reset)
19	PJ1	I	Hi-z	Z	TUN IN DET	Tuner connect detection switch. "L" when tuner is connected.
20	PJ0	O	CMOS	Z	A MUTE H	Audio output ON/OFF (ON when set to low).
21	PD7/HALT	O	cmos	Z	L/M FOR	Control signal of loading motor.
22	PD6/BRQ	O	cmos	Z	L/M REV	

	OFF	Loading	UN-Loading	Brake
L/M FOR	L	H	L	H
L/M REV	L	L	H	H

* Status of port when microprocessor is reset (Z....high impedance)

No.	Pin name	IO	Form	※	Pin function name	Function
23	PD5/BRK	O	cmos	Z	CAM CTL	Camera section DC-DC converter control. "H" when power is turned on.
24	PD4/SYNC	O	cmos	Z	CAM READY	Camera ready signal for serial control. "L" active
25	PD3/C	O	cmos	Z	LIM CONT	Loading motor limit control. "H": Limit ON.
26	PD2/R.W	O	cmos	Z	V CTL-H	Image signal output ON/OFF (ON when it is set to HIGH).
27	PD1/WR	O	cmos	Z	CAM REC-H	Set to HIGH when EE image of camera mode is outputted.
28	PD0/RD	O	cmos	Z	EE-L	Set to LOW when EE image is outputted.
29	PH7	O	Nch	Z	LINE $\overline{\text{IN/OUT}}$	External terminal IN/OUT switching signal. Inputted when it is set to LOW.
30	PH6	O	Nch	Z	PB-L	Circuit is set to PB when set to LOW. PNP transistor required.
31	PH5	O	Nch	Z	EEPROM CS	EEPROM chip select signal.
32	PH4	O	Nch	Z	CASSET LED	S/E sensor detection LED output. Drive when set to HIGH.
33	PH3	O	Nch	Z	D/A CS	D/A converter chip select signal.
34	PH2	O	Nch	Z	ATF CS	ATF IC serial control chip select signal.
35	PH1	O	Nch	Z	OSD STB	Data strobe signal to on-screen display IC.
36	PH0	O	Nch	Z	VIDEO CS	Chip select signal to video signal processing IC.
37	MP	I			MP	Microprocessor mode selection. "L" allows to be fixed to single chip mode. GND
38	RST -	I			$\overline{\text{RESET}}$	Reset input. "L" active.
39	Vss				GND	
40	XTAL	O			XTAL	Crystal oscillator connection terminal for system clock oscillation. Oscillates at 12 about MHz.
41	EXTAL				EXTAL	
42	CS0-	I		Z	SYS 5V	Connected to Vdd.
43	SI0	I		Z	SLV DATA	Camera microprocessor serial data input 1 terminal.
44	SO0	O		Z	SYS DATA I	System control serial data output 1 terminal.
45	SCK0-	IO		Z	$\overline{\text{SLV CLK}}$	Camera microprocessor serial clock input terminal.

* Status of port when microprocessor is set (Z.....high impedance)

No.	Pin name	IO	Form	※	Pin function name	Function
46	PF7/AN11	I	Hi-z	Z	TAPE START	Tape start detection voltage input. A/D input terminal.
47	PF6/AN10	I	Hi-z	Z	TAPE END	Tape end detection voltage input. A/D input terminal.
48	PF5/AN9	I	Hi-z	Z	TUP REEL	Take-up reel pulse input. A/D input terminal.
49	PF4/AN8	I	Hi-z	Z	SUP REEL	Supply reel pulse input. A/D input terminal.
50	AVss				GND	Ground terminal of A/D converter.
51	AVref				SYS 5V	Reference voltage input terminal of A/D converter.
52	AVdd				SYS 5V	Positive power supply terminal of A/D converter.
53	PF3/AN7	I	Hi-z	Z	BATT DET	Battery end/pre-end voltage input. A/D input terminal.
54	PF2/AN6	I	Hi-z	Z	TEST1	Test mode switch input for adjustment. A/D input terminal.
55	PF1/AN5	I	Hi-z	Z	LCD LIGHT	LCD back light service life detection. (A/D input terminal)
56	PF0/AN4	I	Hi-z	Z	KEY 7	Operation key input (7). A/D input terminal. STOP, REW, PB, FF, STILL, etc
57	AN3	I	Hi-z	Z	KEY 5	Operation key input (5). A/D input terminal. Screen adjustment up/down, volume-up/down, etc.
58	AN2	I	Hi-z	Z	KEY 4	REC S/S A/D input terminal.
59	AN1	I	Hi-z	Z	DEW	Dew sensor voltage input. A/D input terminal.
60	AN0	I	Hi-z	Z	ATF ERROR	ATF error (ATF lock error) input. A/D input terminal.
61	PG7/EXI1	I	Hi-z	Z	L/M $\overline{\text{ALARM}}$	LOW is inputted when load of L/M is heavy.
62	PG6/EXI0	I	Hi-z	Z	CLOG	Clog detection signal input. "H" indicates clogged condition.
63	PG5/SYNC1	I	Hi-z	Z	SP/$\overline{\text{LP}}$ DET	SP/LP determination signal input at the time of CUE/REV, etc.
64	PG4/SYNC0	I	Hi-z	Z	C-SYNC IN	Composite synchronizing signal input. Built-in V-SYNC separator.
65	PG3/PBCTL–	I	Hi-z	Z	TEST IN	Confirmation of rate. 16 kHz is outputted from P81 at the time of input at LOW level.

*Status of port when microprocessor is set (Z.....high impedance)

No.	Pin name	IO	Form	※	Pin function name	Function
66	PG2/DPG	I	Hi-z	Z	DRUM PG IN	Drum PG input. FRC capture input terminal.
67	PG1/DFG	I	Hi-z	Z	DRUM FG IN	Drum FG input. FRC capture input terminal.
68	PG0/CFG	I	Hi-z	Z	CAP FG IN	Capstan FG input. FRC capture input terminal.
69	PE7/DAB1	O	cmos	H	LCD PCON-H	LCD power ON/OFF control. "H" when power is turned on.
70	PE6/DAB0	O	cmos	H	DRUM FWD	Drum rotational direction control signal. "H": FWD.
71	PE5/DAA1	O	cmos	Z	(MON)	Test output (terminal for software test).
72	PE4/DAA0	O	cmos	Z	DRUM D/A	DA gate pulse output terminal for drum error output.
73	PE3/PWM1	O	cmos	Z	CAP PWM	PWM output terminal for CAP error output.
74	PE2/PWM0	O	cmos	Z	SP/$\overline{LP}$	HIGH at the time of SP playback.
75	PE1/EC-/INT2	I	Hi-z	Z	CAP FG	CAP FG input terminal for tape counter drive.
76	PE0/INT0	I	cmos	Z	PRINTER-DET.	Printer connection detection terminal. "H" when connected.
77	PI7/SI1	I	Hi-z	Z	EEPROM DI	EEPROM serial input data.
78	PI6/SO1	O	cmos	Z	OSD DATA	OSD serial data output.
79	PI5/SCK1-	O	cmos	Z	$\overline{OSD\ CLOCK}$	OSD serial clock output.
80	PI4/INT1/NM1	I	Hi-z	Z	$\overline{BATT\ OFF}$	Power failure is detected when set to LOW.
81	PI3/T0/DD0	O	cmos	Z	CLOCK OUT	16.384-kHz pulse output when power is ON.
82	PI2/PWM-	O	cmos	Z	TU P-CON	Tuner power source on/off control. "H" when power is ON.
83	PI1/RMC	I	Hi-z	Z	REMOCON IN	Optical remote control signal input.
84	TEX	I			TEX	Crystal connection terminal for 32-kHz timer clock oscillation.
85	TX	O			TX	
86	Vss				GND	Ground terminal.
87	Vdd				SYS 5V	Positive power source supply terminal.
88	NC				SYS 5V	(Connected to Vdd)
89	PA7/PP07/A15	O	cmos	Z	CAP ON	CAP motor ON/OFF control signal. "H": Rotation ON.

* Status of port when microprocessor is set (Z.....high impedance)

No.	Pin name	IO	Form	※	Pin function name	Function	
90	PA6/PP06/A14	O	cmos	Z	CAP FWD	Capstan rotational direction control signal, "H": Normal rotation.	
91	PA5/PP05/A13	O	cmos	Z	DRUM ON	Drum motor ON/OFF control signal, "H": Drum rotated.	
92	PA4/PP04/A12	O	cmos	Z	AV REC-H	When image and sound are recorded. Recording when set to "H".	
93	PA3/PP03/A11	O	cmos	Z	ROT ERASE	Rotary erase oscillation on/off signal. Oscillating when set to "H".	
94	PA2/PP02/A10	O	cmos	Z	PREC-H	ATF-IC pilot REC/PB switching signal. Recording when set to "H".	
95	PA1/PP01/A9	O	cmos	Z	SCLOCK	Serial clock to peripheral IC.	Data to EEPROM, D/A, ATF Y/C.
96	PA0/PP00/A8	O	cmos	Z	SDATA	Serial data to peripheral IC.	
97	PB7/PP015/A7	O	cmos	Z	SEL 2	Selection of frequency for ATF REF pilot signal.	
98	PB6/PP014/A6	O	cmos	Z	SEL 1	f_1 f_2 f_3 f_4 SEL 1/ H L H L SEL 2/ H H L L	
99	PB5/PP013/A5	O	cmos	Z	H-AMP-SW	H-SW 15-Hz signal (for servo test).	
100	PB4/PP012/A4	O	cmos	Z	LCD RVS	Switching of LCD for face-to-face shooting mode. "H": Normal operation.	

Status of each port at power source off

No.	IO	Pin function name	※
1	O	H-SW-P	L
2	O	JOG	L
3	O	JOG VD H	L
4	O	WH	L
5	O	REF30Hz	L
6	O	P-CON-H	L
7	I	ME/$\overline{MP}$	Z
8	I	TURN SW	Z
9	I	PROTECT SW	Z
10	I	SW-C	Z
11	I	SW-B	Z
12	I	SW-A	Z
13	I	CAMERA SW	Z
14	I	EJECT SW	Z
15	I	VCR SW	Z
16	I	CASCON SW	Z
17	I	VCR ADJ	Z
18	I	CAM ADJ	Z
19	I	TUN-IN-DET	Z
20	O	A MUTE-H	L
21	O	L/M FOR	L
22	O	L/M REV	L
23	O	CAM CTL	L
24	O	CAM READY	L
25	O	LIM CONT	L
26	O	V CTL-H	L
27	O	CAM REC-H	L
28	O	EE-L	L
29	O	LINE IN/OT	*H
30	O	PB-L	*H
31	O	EEPROM CS	*H
32	O	CASSET LED	*H
33	O	D/A CS	*H
34	O	ATF CS	*H
35	O	OSD STB	*H
36	O	VIDEO CS	*H
37	I	MP	L
38	I	$\overline{RESET}$	Z
39		GND	
40	O	XTAL	
41	I	EXTAL	
42	I	SYS 5V	Z
43	I	SLV DATA	Z
44	O	SYS DATA 1	Z
45	IO	$\overline{SLV\ CLK}$	Z
46	I	TAPE START	Z
47	I	TAPE END	Z
48	I	TUP REEL	Z
49	I	SUP REEL	Z
50		GND	
51		SYS 5V	
52		SYS 5V	
53	I	BATT DET	Z
54	I	TEST 1	Z
55	I	LCD LIGHT	Z
56	I	KEY 7	Z
57	I	KEY 5	Z
58	I	KEY 4	Z
59	I	DEW	Z
60	I	ATF ERROR	Z
61	I	L/M $\overline{ALARM}$	Z
62	I	CLOG	Z
63	I	SP/$\overline{LP}$ DET	Z
64	I	C-SYNC IN	Z
65	I	TEST IN	Z
66	I	DRUM PG IN	Z
67	I	DRUM FG IN	Z
68	I	CAP FG IN	Z
69	O	LCD PCON-H	L
70	O	DRUM FWD	L
71	O	(MON)	L
72	O	DRUM D/A	L
73	O	CAP PWM	L
74	O	SP/$\overline{LP}$	L
75	I	CAP FG	Z
76	I	(SYS 5V)	H
77	I	EEPROM DI	Z
78	O	OSD DATA	Z
79	O	$\overline{OSD\ CLOCK}$	L
80	I	$\overline{BATT\ OFF}$	Z
81	O	CLOCK OUT	L
82	O	TU P-CON	L
83	I	REMOCON IN	Z
84	I	TEX	
85	O	TX	
86		GND	
87		SYS 5V	
88		SYS 5V	
89	O	CAP ON	L
90	O	CAP FWD	L
91	O	DRUM ON	L
92	O	AV REC-H	L
93	O	ROT ERASE	L
94	O	PREC-H	L
95	O	SCLOCK	L
96	O	SDATA	L
97	O	SEL 2	L
98	O	SEL 1	L
99	O	H-AMP-SW	L
100	O	LCD RVS	L

① The input port should be fixed to LOW by using an external circuit.

★ Floating port may cause lithium backup electric current to increase.

② *H indicates that N-ch is open.

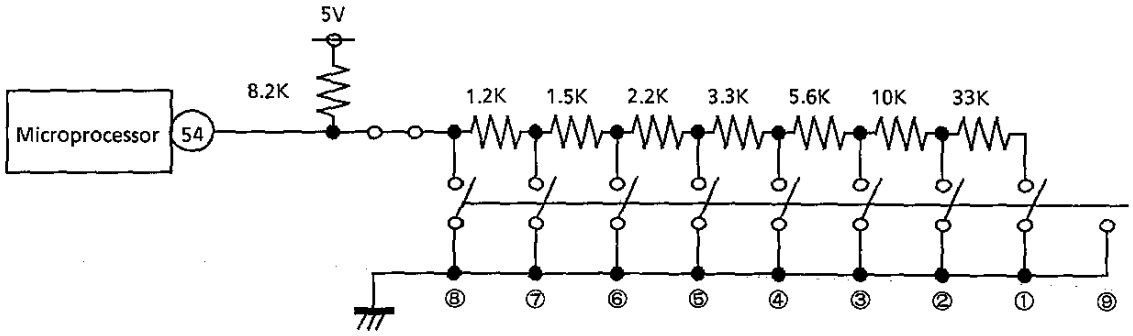
14-2. Pin input/output

14-2-1. A/D converter

The A/D converter built in the microprocessor is used to read the following signals.

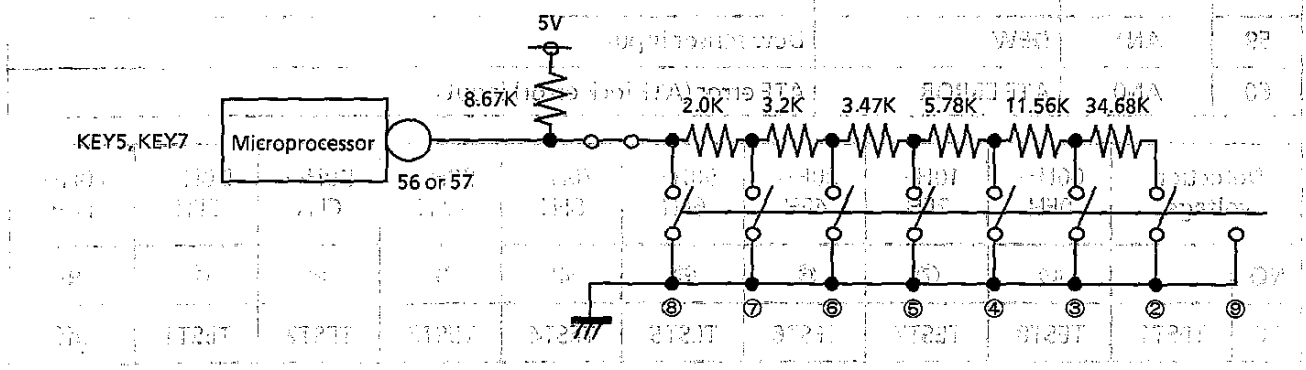
No.	Port	Port name	Function
46	AN11	TAPE START	Tape start sensor
47	AN10	TAPE END	Tape end sensor
48	AN9	TUP REEL	Take-up reel pulse input
49	AN8	SUP REEL	Supply reel pulse input
53	AN7	BATT DET	Battery voltage detection
54	AN6	TEST1	Test mode setting
55	AN5	LCD LIGHT	LCD back light service life detection
56	AN4	KEY 7	Control key input (7) LCD display's W function keys STOP, REW, PB, FF, STILL/DIS, SCENE ADJ, etc.
57	AN3	KEY 5	Control key input (5) MENU ON/OFF, SELECT, SET, AV-SELECT, UP, DOWN
58	AN2	KEY 4	REC S/S (rubber switch compatible)
59	AN1	DEW	Dew sensor input
60	AN0	ATF ERROR	ATF error (ATF lock error) input

Detection voltage		00H~ 0FH	10H~ 2FH	30H~ 4FH	50H~ 6FH	70H~ 8FH	90H~ AFH	B0H~ CFH	D0H~ EFH	F0H~ FFH
NO		⑧	⑦	⑥	⑤	④	③	②	①	⑨
56	TEST1	TEST8	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	off



Detection voltage		00H~ 17H	18H~ 47H	48H~ 6FH	70H~ 8FH	90H~ AFH	B0H~ CFH	D0H~ EFH	F0H~ FFH
NO		⑧	⑦	⑥	⑤	④	③	②	⑨
56	KEY7	—	REW	PB	FF	STOP	STILL	MODE	off
		VCR						DISPLAY	
		INDEX SEARCH	SNAP	DGTL EFCT	DIS	SCENE MENU	FOCUS		
		CAM				SCENE MENU	FOCUS ※1		
			CAMERA SEARCH REVERSE		CAMERA SEARCH FOR-WARD			←(At display off)	
57	KEY 5		—Menu—			—AV—			
		SET Counter reset	SELECT Counter memory	ON/OFF	UP (▲)	DOWN (▼)	SELECT	—	off

※1 When not provided with the digital function



(1) MENU ON/OFF/SELECT/SET

The menu key is used to turn on and off the menu. With this key on, the menu items can be reprogrammed using the SELECT and SET keys.

For menu control, take the following steps.

1) Press the MENU key to turn on the menu display.
2) Select an item to be modified with the SELECT key. (Move the cursor to the item.)
3) Press the SET key to change entries
4) Using the SET key, modify the entry to a desired value.
5) To set the clock:
   - Numbers go up with the SELECT key. Enter the data with the SET key.
   - When the last item has been set;

     JAPAN: The cursor moves to the date display.

     OTHERS: The move stays in the same position.
6) For other items to be modified, take the steps from 2) on again.
7) Finally press the MENU key to clear the menu. (The menu will be automatically cleared in 5 seconds if any menu-related key is pressed.)

The items listed below can be set on the menu.

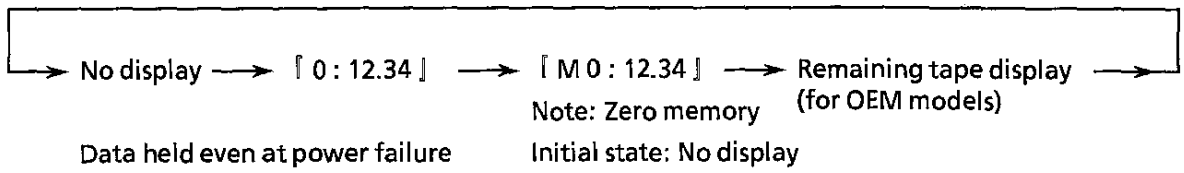
	Item	Contents
Camera	Date/Time display	Off/Auto/On
	Date/Time select	Date + Time/Date
	Date/Time Setting	Year/Month/Day/ Hour/Minute
	Self record	Auto/Off
	Screen	Normal/Wide
	Remote control	On/Off ①

	Item	Contents
VCR	AV in/out	Output/Input ②③
	Edit	On/Off
	Remote control	On/Off ①

① This item is available commonly in camera/VCR mode.
② This item is not available for Europe-destined models.
③ This item will not be used after the tuner connection.

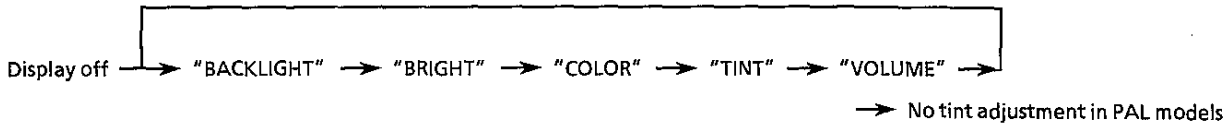
Notes

- The menu display is not available in any other mode than the EE screen as well as during recording. The display is automatically cleared if the prohibition condition is brought about.
- When turned on, the menu starts from the one in the same mode. The camera-mode menu, however, starts with the Date/Time setting item if the Date/Time has not been set yet.
  Every time the MENU SELECT key is pressed with the menu off, the counter display changes as follows.



When the counter display is on with the menu off, pressing the MENU SET key sets the counter to "0:00:00".

(2) AV SELECT key
This key is used to select LCD picture, sound and other adjustment items.
Camera mode/VCR mode
The adjustment items change as follows.



Once the AV SELECT key has been pressed, the adjustment items and their contents are displayed.

- The display will disappear if any key is not pressed within 4 seconds.
- The selected adjustment item is held for 10 seconds after the display has appeared.
  When the AV SELECT key is pressed again within 10 seconds after the display's disappearance, the item just before is displayed.

If the data has been already modified, the new data is written in the EEPROM.
The modified contents of the adjustment item are also written in the EEPROM.
(If the power is turned off within 10 seconds or the picture adjustment is called, the data is written in the EEPROM at the moment.)

(5) CAM ADJ

- This terminal is used to detect that the camera is in the automatic adjustment mode.
- The terminal should be triggered even if the microprocessor is reset with this terminal at low level.
- The automatic camera adjustment mode is called up when this terminal gets low.
- This mode is brought about from the power-off state.
  At this time, the rec pause mode is called.
- Once turned on, the power is kept on even when this terminal gets high. The power should be turned off, however, when the CAMERA/OFF/VCR switch is off.
- This function is not effective at power failure.

(6) VCR ADJ

- This terminal is used to detect that the VCR is in the automatic adjustment mode.
- The terminal should be triggered even if the microprocessor is reset with this terminal at low level.
- The system controller power and the camera power are turned on when this terminal gets low. Now the adjustment mode is picked up according to the command.
- Once turned on, the power is kept on even when this terminal gets high. The power should be turned off, however, when the CAMERA/OFF/VCR switch is off.
- This function is not effective at power failure.

14-2-3. Other key input sections

(1) PROTECT switch

This switch is used not to wrongly erase the tape. The unit is not ready to make recording.

(2) ME/$\overline{MP}$

This terminal is used to identify ME and MP tapes. ME tapes are identified when the terminal gets high.
The internal flag is established to switch on and off the ATF gain (servo).

(3) Mechanism switches A, B and C

The mechanism position is detected according to the switch positioned as listed below. Reading is made after 2-time matching at 2.7 msec cycle.

Mechanism mode	SW			Contents
	A	B	C	
BLANK	H	H	H	Position not fixed.
END	H	H	L	T hard brake cleared.
EJECT	H	L	L	Cassette control up.
USE	H	L	H	(Unskewed end) cassette control down ready.
LOAD	H	L	L	Middle point. Drum from reverse to forward.
READY	L	L	H	Pinch roller off, tension regulator off.
TURN	L	H	H	Pinch roller off, tension regulator on.
R/P	L	H	L	Pinch roller on, tension regulator on.
FF	L	L	L	Pinch roller on, tension regulator semi-on.

(4) PRINTER DET

This terminal is used to detect the printer connection.
The connection is identified when the terminal gets high.
The image from the printer, when connected, is projected on the LCD even when the unit is in the play or special play mode. To cope with noises caused in the special play mode, however, the control pulse is outputted from the WH terminal. This pulse in turn causes disturbance to the image. To avoid this, the WHterminal is forced to be at "H" level (at power on).

14-3. EEPROM control

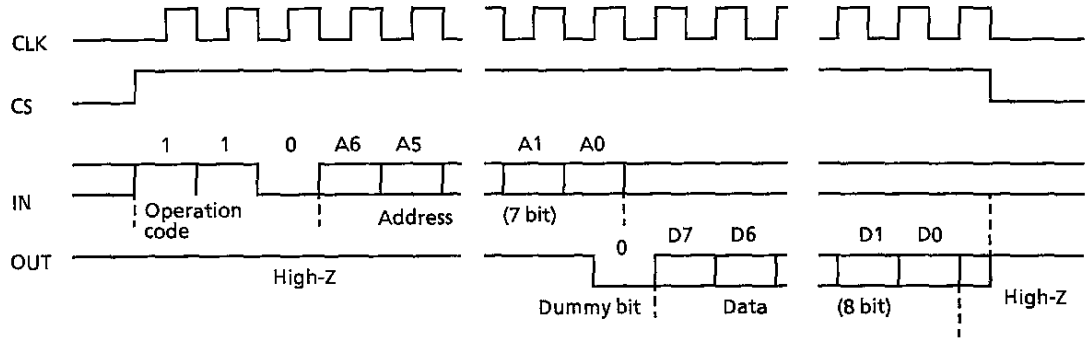
To handle the automatic VCR adjustment, a connection can be made between an EEPROM and a D/A converter.

14-3-1. Instruction timings

<READ>

The READ instruction is used to read the contents of a specified memory address. The read data is serially outputted to the DO pin. Once the instruction is confirmed, the dummy bit (logic "0") first goes out of the output pin.

(Timing chart)

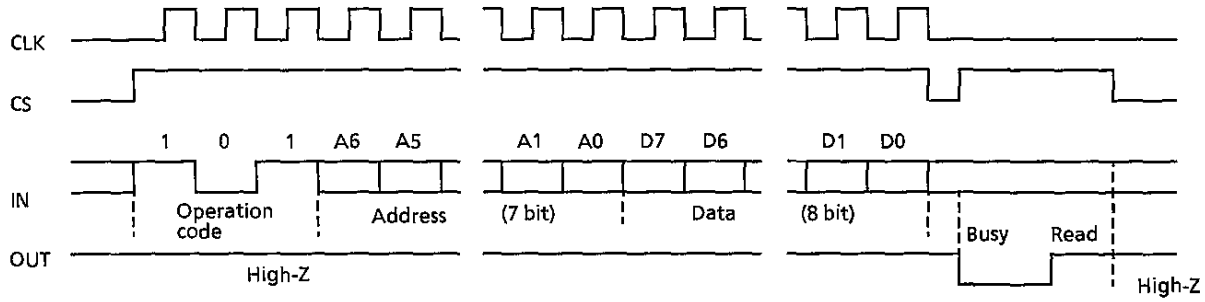


<WRITE>

When the WRITE instruction with 8-bit data is put in, the CS signal comes to low level (250 nsec later). The DO pin provides for status display. This pin is kept at low level during programming and gets high after the data is written to the register of a designated address.

This instruction first erases the data that are already stored at the designated address and then writes new data. It is therefore unnecessary to execute any ERASE instruction.

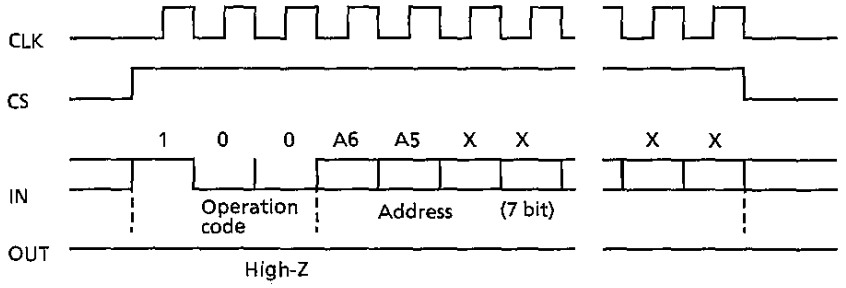
(Timing chart)



<EWEN/EWDS>

It is needed to execute the EWEN (ERASE/WRITE ENABLE) instruction after turning on the power and before carrying the PROGRAM instruction. Once this step is made, the status remains until the EWDS (ERASE/WRITE DISABLE) instruction is introduced.

(Timing chart)



	A6	A5
EWEN	1	1
EWDS	0	0

14-3-2. EEPROM data setting

Addr	DATA	Contents			Type
00	Version number	(Main) ROM version			System codes
01		(Sub)			
02	Destination code	(Main) By destinations	*A "00": Original: JAPAN		
03		(Sub)			
04	Specification code	(Main) Mainly for OEM	*B "00": Original		
05		(Sub)			
06	Menu select code	(Main) Mainly for OEM	*C "00": Original		
07		(Sub)			
08	Soft select code	(Main) Debug/Service	*D "00": Original		
09		(Sub)			
0A	meka swp	(Main) H-SW-P adjustment			VCR automatic adjustment
0B		(Sub)			
0C	bat ref	(Main) Battery shut-off adjustment			
0D		(Sub)			
0E	calendar	(Main) Initial year for date setting	"93": Original		At soft select
0F		(Sub)			
10		(Initial data: Voltage)			D/A-1 output data
11	DEV-ADJ	Deviation adjustment	Output to D/A-1's A01	80h	
12	FILT-ADJ	Filter fo adjustment	Output to D/A-1's A02	80h	
13	VOL CTL	Sound volume	Output to D/A-1's A03	FFh	
14	EE ADJ	EE level adjustment	Output to D/A-1's A04	60h.	
15	PHASE ADJ	Comb filter (Phase) adj.	Output to D/A-1's A05	80h.	
16	COMB ADJ	Comb filter (Gain) adj.	Output to D/A-1's A06	80h.	
17	EMPH ADJ	Preemphasis input level adj.	Output to D/A-1's A07	80h.	
18	CARR ADJ	Y FM carrier adj.	Output to D/A-1's A08	80h.	
19	DEV ADJ	Y FM deviation adj.	Output to D/A-1's A09	60h.	
1A	REC Y ADJ	REC Y level adjustment	Output to D/A-1's A10	80h.	
1B	REC C ADJ	REC C level adjustment	Output to D/A-1's A11	70h.	
1C	PB ADJ	Video PB level adjustment	Output to D/A-1's A12	80h.	
1D	DC 1/2	Dark clip level modification			Y/C serial data change
1E	FBCL 1/2	Chroma feedback comb loop gain modification			
1F	NCL 1/2	NC characteristic modification			
20	(Spare)				D/A-2 output data
21	TINT CTL	LCD Tint Control Voltage	Output to D/A-2's A01	80h	
22	COLOR CTL	LCD Color Control Voltage	Output to D/A-2's A02	80h	
23	R-WB ADJ	White balance (red) adj.	Output to D/A-2's A03	80h	
24	CONTRAST ADJ	Contrast adj.	Output to D/A-2's A04	80h	
25	Back Light CTL	LCD Back Light Control Voltage	Output to D/A-2's A05	FFh	
26	BRIGHT CTL	LCD Bright Control Voltage	Output to D/A-2's A06	80h	

Addr	DATA	Contents		Type
27	VCO ADJ	VCO adj. Output to D/A-2's A07	80h	D/A-2 output data
28	B-WB ADJ	White balance (blue) adj. Output to D/A-2's A08	80h	
29	SP CONT-H	Speaker Control Voltage Output to D/A-2's A09	00h	
2A	EDIT-H	Output to D/A-2's A10	00h	
2B	COM-BIAS ADJ	Common bias adj. Output to D/A-2's A11	80h	
2C	H-POSI ADJ	Horizontal position adj. Output to D/A-2's A12	80h	
2D	(Spare)			
2E	BL CTL-L	Back light brightness control voltage. Normal-mode voltage.	8Ah 2.7V	Brightness voltage modification
2F	BL CTL-H	Back light brightness control voltage. Bright-mode voltage.	CCh 4.0V	
30	(Spare)			
31	BL DET-L	Back light service life detection voltage. Minimum voltage.	50h 1.5V	Detection voltage modification
32	BL DET-H	Back light service life detection voltage. Maximum voltage.	FAh 4.7V	
33	(Spare)			
34				
35				
36				
37				
38	OPE TIME (1) L	Drum motor operating time total Unit: seconds (0-FFFFFF: Max. 16.77 million sec. = 4660 hours)		
39	OPE TIME (1) M			
3A	OPE TIME (1) H			
3B	OPE TIME (2) L	Capstan motor operating time total Unit: seconds (0-FFFFFF: Max. 16.77 million sec. = 4660 hours)		
3C	OPE TIME (2) M			
3D	OPE TIME (2) H			
3E	EJECT CNT L	Cassette ejection frequency Unit: times (Max. 65535 ejections)		
3F	EJECT CNT H			
40 ↓ 7F	Not determined			

Notes:

- Addr 00-0F data is inputted and judged only at resetting.
- Addr 10-2F data is judged as "not adjusted" at FF.
  The preset initial value is adopted instead.
- The "Sub" data is made by bit-inverting the "Main" data.
  When reading, remove the EXOR of both the Main and Sub data. If FF is not achieved, ignore the data. In such a case, set the initial values of "meka swp" and "bat ref" in the RAM.
- The output to D/A converters should be made after the PCON gets started. The output should begin and end during the video mute.

14-4. D/A converter control

The data is outputted from the D/A converter through serial transfer.

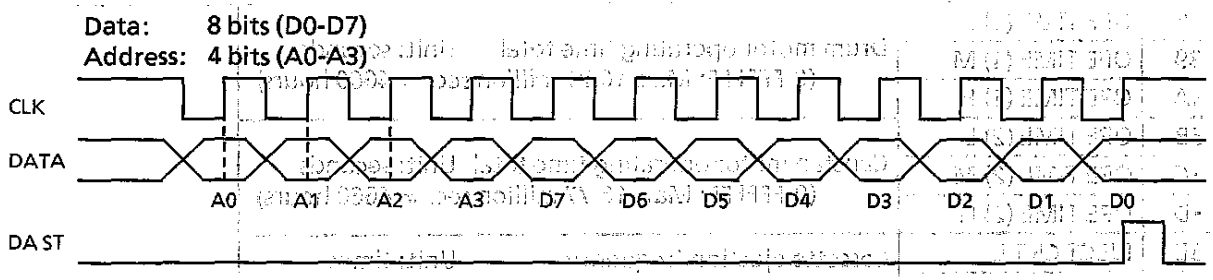
D/A converter output table (1) IC5401 (Y/C)

ADR	Function	Initial value
AO 1	DEV-ADJ	80h V
2	FILT-ADJ	80h V
3	VOL CTL	FFh V
4	EE ADJ	60h V
5	PHASE ADJ	80h V
6	COMB ADJ	80h V
7	EMPH ADJ	80h V
8	CARR ADJ	80h V
9	DEV ADJ	60h V
10	REC Y ADJ	80h V
11	REC C ADJ	70h V
12	PB ADJ	80h V

D/A converter output table (2) IC807 (LCD)

ADR	Function	Initial value	
AO 1	TINT CTL	80h V	
2	COLOR CTL	80h V	
3	R-WB ADJ	80h V	
4	CONTRAST ADJ	80h V	
5	BackLight CTL	FFh V	*1
6	BRIGHT CTL	80h V	
7	VCO ADJ	80h V	
8	B-WB ADJ	80h V	
9	SP CONT-H	00h V	
10	EDIT-H	00h V	
11	COM-BIAS ADJ	80h V	
11	H-POSI ADJ	80h V	

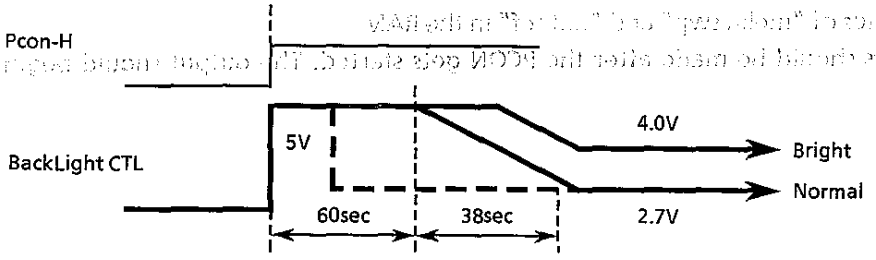
[Timing chart]



*1 · · · Back light control (brightness control)

The back light brightness is controlled with the voltage coming from the D/A converter.

1. To improve the light-up performance, 5V (data FF) is forced to go out for 60 seconds after the power is turned on.
2. Then the voltage is reduced in about 30 seconds until the normal (2.7V) or bright (4.0V) setting is made according to the AV selection.
3. While the 5V forced output is made (in Step 1 above), the normal (2.7V) setting is immediately introduced in the following cases.
   ① When an automatic adjustment command is received
   ② When the battery shut-down inspection mode is called up by the remote controller.



14-5. Data transfer with dedicated tuner

The bus line two-way data transfer system is intended to operate the LCD Movie with peripheral equipment in a broader way. A single signal line is used for data communication with optional equipment.
The MS Movie Bus Line (called MS-BUS) will be further developed as a compact external bus. With the Movie as the master communication unit, the following conditions are considered.

14-5-1. MS bus line standardization factors

(1) The Movie's system control program is not be modified.
(2) No dedicated hardware is added for the MS-BUS (an interface only added).
(3) General-purpose input/output ports of the microprocessor are used for the MS-BUS. (No port conditions which would limit the applicable types of microprocessor is added.)
(4) The MS-BUS consists of a single signal line.
(5) No cost increase is expected for the Movie as well as its peripheral equipment.

[Transfer points]

(1) The VCR system controller, used as the transfer master, determines the transfer start timing.
(2) Hand-shake type two-way transfer is adopted with one unit of 44 msec (32-cycle process on the system controller).
(3) The data is carried on the pulse width-modulated signal. Logic "1" or "0" is identified during the period from the leading edge to the "L" level.

[Limitations]

(4) Transfer speed is as low as about 360 bps.
(Comparative reference: LANC = 9600 bps, remote control transmitter = 117 bps)
For this reason, some limitations are expected when a task requires higher processing speed or processing accuracy (editing, for example).
(5) The entire system shall be formed with Sharp-made or compatible peripherals, which is related to the LCD Movie.

14-5-2. Transfer format between system control and tuner

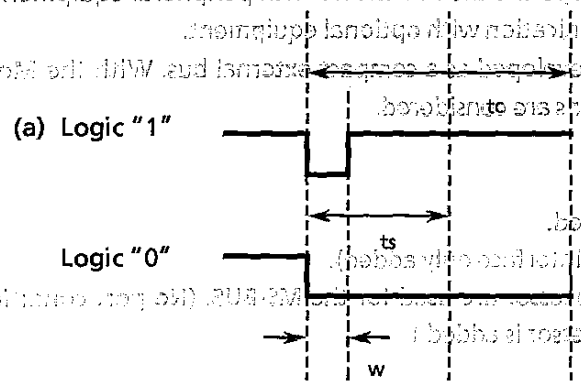
(1) Specifications
  (a) Transfer speed
  366 bps (typical) (16-bit data exchange every 44 msec)
  (b) Transfer system
  Start-stop synchronization: Open-collector type two-way serial communication
  Data length: 16 bits
  Serial data: Transfer through MSB
  (c) Error detection
  Odd parity system
  A sum check bit is set so that an odd number of "1"'s be produced from the total of 11 bits: 3 command bits and 8data bits.

(2) Interface timing

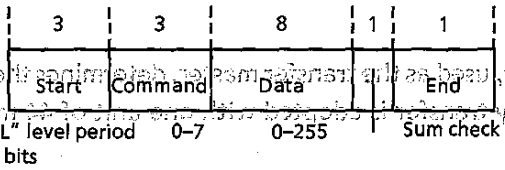
[Logic judgment]
Level at the time "ts" since the leading edge

0.1ms ≦ w < 0.68ms
1.36ms ≦ ts < 2.1ms
2.72ms ≦ tc < 5.4ms

(Reference)
The Movie system controller handles 1.36 msec as the reference clock.



(b) Frame composition



The start bit is for frame synchronization and the "L" level period lasts for 3 bits.
The end bit is for triggering the frame synchronization and the logic "1" is fed out.

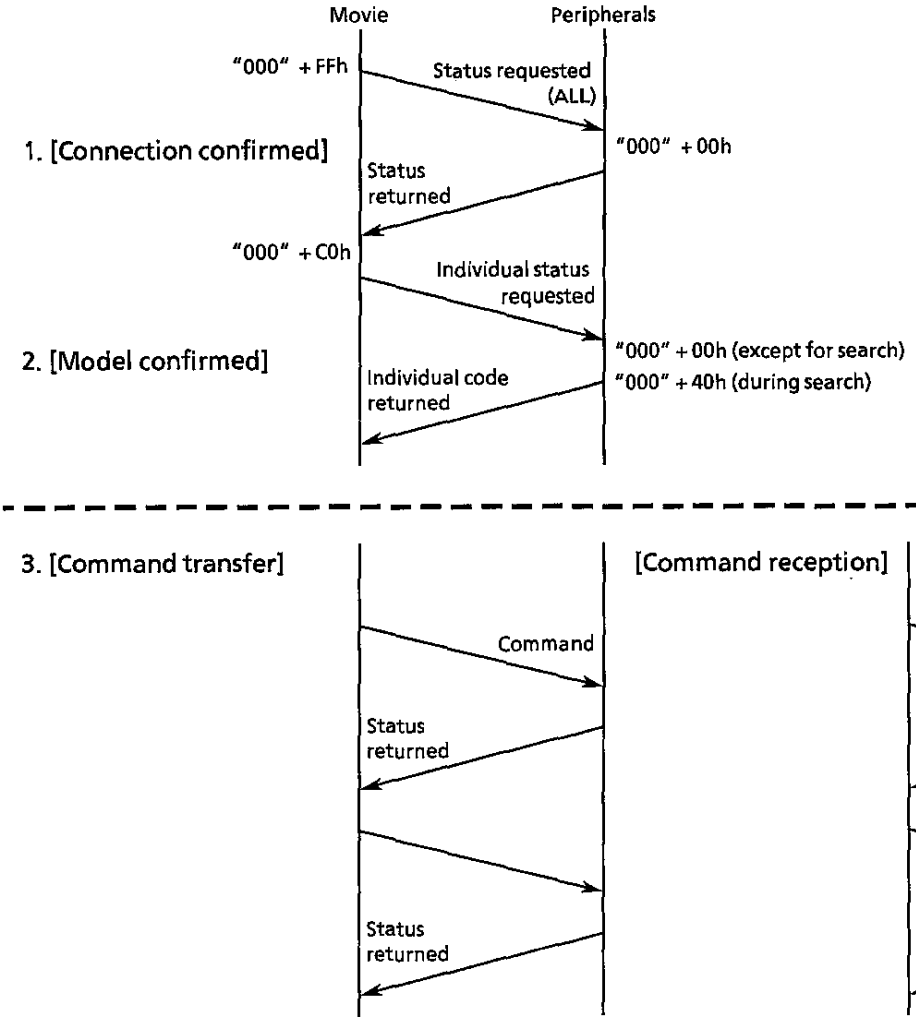
(c) Transfer sequence

- The system controller puts out the start bit.
- The input and output are switched every frame (except for the burst transfer).

(Type)	Start	Command + data	Start	Command + data	Start	Command + data	Start	Command + data
(Direction)	From system controller	From system controller	From system controller	To system controller	From system controller	From system controller	From system controller	To system controller

(3) Typical protocol

The Movie checks a unit being connected. The communication protocol for data transfer is as follows.



14-6. Error messages

The following symbol and codes appear on the counter display of the monitor, if any of the sensors is activated, to tell the types of troubles.

Symbol/code	Trouble
E007	No input is given from the capstan frequency generator for 1 second.
E011	The loading motor runs in normal direction for longer than 5 (or 10) seconds, but the next mode is not brought about.
E012	The loading motor runs in reverse direction for longer than 5 (or 10) seconds, but the next mode is not brought about.
⏏ or EJECT	In any of the E020, E025 and E026 errors below, it is displayed with the STOP key held down for 3 seconds. The error is cleared when ejection is complete.
E020	The speed is not locked for 6 seconds. To be cleared when the speed is locked.
E025	The take-up reel sensor is activated.
E026	The supply reel sensor is activated.

15. Y/C SIGNAL PROCESSING CIRCUIT (PAL)

* Refer to the VL-MX series manual for details of the 8mm video standard.

<Video Circuit (PAL) of Models VL-E30S/H/X, E7E/D, E40S/H/X, E8E/D>

A single-chip Y/C circuit CXA1700R is employed for the E30/E40 series models. Its major functions and the signal flows in the video system are discussed below.

15-1. Functions of the main signal processing IC (IC401: CXA1700R)

(1)	Input/output functions	Switching of input signal for two lines
		Video AGC
		Sync separation
		Y/C mixing, 75-ohm video output driver
		Y/C separation comb filter
		Y signal H correlation detection
(2)	Y line functions	Y preemphasis/deemphasis
		White/dark clip
		Clip compensation
		HHS/HHS cancellation
		Y FM modulation/demodulation
		Y dropout compensation
		Y/C crosstalk removal
(3)	C line functions	ACC
		C emphasis/deemphasis
		Burst emphasis/deemphasis
		XO/VXO
		APC/AFC
		APC ID/AFC ID/Burst ID
		ACK
		APC correction
		HHK
		PI/PS
		Frequency conversion system
		PB C BPF/REC C LPF
		PB C LPF/Carrier BPF

* Switching and characteristics change in the IC are controlled by serial data (32 bits).

15-2. Signal Processing Paths

(1) Flow of camera EE signal

The Y signal output from the camera PWB (CAM Y) is supplied to pin (11) of connector SC702 of the VCR PWB, and then to pin (11) of IC1402 (NJM2285M). Here the recording characters, such as date and time, are combined with the border lines of the characters and fed out of pin (5).

The CAM Y signal is inputted to pin (30) of IC401 (CXA1700R) and fed to the 75-ohm driver line of the Y/C mixing amplifier when the video AGC is turned off (serial data 29 bits: L). The path is the line from the output pin (34) of IC401 to the input pin (32) of IC401.

On the other hand, the C (CAM C) signal going from the camera PWB is supplied to pin (13) of connector SC702 (VCR PWB)and fed to pin (16) of IC1402. Here the chroma signal is muted only in the range containing characters so that no color component is mixed with the recording characters.

The CAM C outputted from pin (3) of IC1402, passing through Q433, is fed to pin (64) of IC401 and then to the Y/C mixing amplifier's 75-ohm driver line.
The resulting signal is fed out of pin (36) of IC401 and supplied to the AV box via pin (4) of SC601.

(2) Flow of camera record Y signal

The camera record Y signal is carried to pin (30) of IC401 along the same path as the camera EE (Y) signal and branched into the EE path and the record path inthe IC.
The signal, passing through the video AGC in the off mode, is fed to the equalizer block (fsc trap and Y low-pass filter) and out of pin (14) of IC401.
The output signal from pin (14) of IC401 is further fed to the equalizer Q409 of the external circuit, and is corrected in phase generated in the IC. It passes through Q412 and enters pin (5) of IC401 with the level of emphasis input which has been adjusted at pins (5), (6) and (7) of IC403 (BA7655AF).
The input signal from pin (5) of IC401, passing through the preemphasis circuit composed of the main emphasis and subemphasis, is white/dark-clipped (preset value: white clip 220% and dark clip 100%). The emphasis circuit refers to a circuit to emphasize the high-frequency band, and the high-frequency band is attenuated (deemphasized) in playback, thereby improving the signal-to-noise ratio without degrading the details information. As for clipping, the spike generated in the emphasis is cut at a specified level (controlling an over-modulation in the FM circuit) to suppress the inversion phenomenon in playback.
The clipped signal, further passing through the smear correction circuit, is subjected to carrier adjustment (sync tip: 4.2 MHz) and deviation adjustment (between the sync tip and white peak: 1.2 MHz). Then it passes through the HHS (Half H Shift) circuit where the FM frequency of the odd-numbered field's signal is carrier-shifted by 1/2H in order to reduce the crosstalk of adjacent tracks.
Thus the FM-modulated signal is fed out of pin (39) of IC401.
The Y-FM signal, passing through Q3404, has the side band component near 732 kHz/1.5 MHz removed by the low-frequency chroma trap and AFM trap, and is fed through the equalizer (Q3405) to correct the FM waveform distortion and sent out to the head amplifier with the recording current optimized at pins (5), (6) and (7) of IC3401 (BA7655AF).

(3) Flow of camera record C signal

The camera record C signal, proceeding along the same path as the camera EE (C) signal until it goes out of pin (3) of IC1402, is fed to pin (53) of IC401.
In camera recording, the interior of the IC is in the S-REC mode (serial data 31 bits: H) and C-SEL normal mode (serial data 8 bits: L); therefore the C signal, after passing through the chroma band-pass filter, enters the ACC amplifier. This signal, of which the burst level is fixed by the ACC amplifier, is subjected to chroma emphasis (side band emphasis) and burst emphasis (burst up 6 dB) proper to the 8mm VCRs, and converted to low-frequency band (4.433619 MHz to 732.42 kHz). The 8mm VCR uses a multiple-frequency recording system, and the low-frequency conversion chroma side band is easily affected by the pilot signal and the audio signal. To cope with this, in recording, the side band is emphasized around 4.433619 MHz in modulation, and then attenuated after demodulation in playback to recover its original condition. Chroma emphasis thus contributes to an improvement in signal-to-noise ratio as the Y emphasis does.
Further, PS (Phase Shift) processing is performed in order to reduce the crosstalk from adjacent tracks in low-frequency band conversion. PS processing is to shift the phase of color signal in recording by 90 degrees in every 1H after the low-frequency band conversion. The rotation direction in shifting the phase should be opposite to each other in neighboring tracks.

In playback, the phase is returned to the original and combined with the playback signal 1H behind. As a result, necessary signal is enlarged through synthesization with the noise-to-signal ratio improved, and unnecessary crosstalk is canceled. The chroma signal converted to the low-frequency band enters the block of record C low-pass filter, where the sum components in balanced modulation and noise components in the audio band are removed. (When a signal without burst is inputted, it is muted by the following ACK switch.)

The low-frequency band conversion chroma signal passing the low-pass filter is outputted from pin (8) of IC401 and sent out to the head amplifier with the recording current optimized at pins (1), (2) and (3) of IC3401.

(4) Flow of composite record signal (external input) (VL-E30X, E40X, E7E/D, E8E/D)

The externally inputted signal is supplied from the AV box to pin (4) of SC601 on the main PWB, terminated at a 75-ohm impedance, then fed to pin (28) of IC401. The input signal flows on when the video AGC is turned on (serial data 29 bits: H) and the S-REC mode is turned off (serial data 31 bits: H), and the signal 2H behind is added or subtracted inside the IC, and the Y/C signal is separated.

The signal in the 1H/2H delay lines is fed out of pin (23) of IC401 as a signal for delay line, and fed to pin (2) of IC402 (1HY/2H CCD).

The 2H-delayed signal is fed out of pin (7) of IC402 (1H/2H CCD), and enters FL401 via the buffer Q403 so that the noise above the secondary harmonic components is reduced the. The delayed signal with the noise reduced is matched in phase with the signal 2H behind in Q404, and amplified in Q405, by which the input level at pin (21) of IC401 is brought up to the specified value. Inside the IC, it is subjected to gain adjustment with the main signal, and Y/C separation is performed. The Y signal which is Y/C-separated passes through the equalizer and adds the fsc trap to the chroma component separated in order to supplement the $f_H/2$ component of the Y signal removed by the comb filter. It is mixed with the Y signal. The Y signal proceeds along the same path as the camera record (Y) signal and is fed to the equalizer block (fsc trap and Y low-pass filter). The C signal is completed when the gain adjustment of Y/C separation is finished, and proceeds to the chroma band-pass filter by the same path as the camera record (C) signal.

(5) Flow of playback C signal

The mixed FM wave (PB-Y RF), passing the RF AGC block from the head amplifier, is provided with the AFM trap (1.5 MHz), chroma trap (732 kHz), and secondary harmonic trap around Q3401 and is deprived of components other than the Y component. Further the PB-Y FM signal is inputted to the soft limiter circuit Q3402 and corrected in harmonic characteristics. This circuit serves to correct the balance of the lower wave and upper wave of the Y FM signal, thus preventing the inversion phenomenon.

The signal coming out of Q3402 is inputted to pin (41) of IC401, of which the FM level is adjusted by the limiter. Then the demodulated signal passes through the low-pass filter and is outputted from pin (7).

The signal coming out of pin (7) is shaped in the waveform by the equalizer consisting of Q417 and Q416 and by the peaking amplifier, and inputted to pin (1) of IC403.

The signal out of pin (3) of IC403 is fed to pin (10) of IC401 via Q435, and is adjusted in IC403, so that TP405 (Video OUT) has 2.0 Vp-p (alignment tape playback). This is because the video output level of the playback Y signal is determined by the input level at pin (10) of IC401.

The signal thus coming into pin (10) of IC401 is subjected to deemphasis (high-frequency attenuation circuit) and HHS cancellation (Half H Shift Cancel), and flows to the crosstalk removing circuit and the dropout correction circuit. The deemphasis circuit feeds back the signal emphasized in the high-frequency band in the emphasis circuit in recording to its original condition, and the HHS cancellation circuit returns the DC level difference in every field due to the carrier shifting recording to its original condition.

The correction signal of crosstalk/dropout, branched off the main signal, is mixed with the chroma signal and fed to the 1H/2H delay lines, and finally goes out of pin (23) of IC401. (The chroma signal also enters the delay line for removal of crosstalk of adjacent tracks.)

The correction signal, flowing along the same path as that of Y/C separation, is fed out of pin (5) of IC402 (1H output). The 1H-delayed signal, passing through the amplifier Q420, is fed to FL402 for reducing the noise above the secondary harmonic component. The 1H-delayed signal with the noise reduced returns to pin (19) of IC401 via the buffer Q419.

The correction signal has its chroma component removed by the fsc trap in the IC. becomes a Y signal 1H delayed, and is subtracted from the signal 1H behind (Y signal branched from the main signal), thereby the crosstalk component being extracted. The crosstalk component is attenuated and then subtracted from the main signal, by which the crosstalk is removed. Further the Y signal 1H behind returning from the delay line substitutes the main signal in dropout, thereby compensating missing signals.

The Y signal with the crosstalk removed, passing through the equalizer block (sharpness correction, fsc trap), is fed out of pin (14) of IC401. The output signal passes through Q409 (equalizer) and Q412 (peaking amplifier). The peaking amplifier raises the high-frequency band in playback to improve the sharpness of the images.

The signal out of Q412, passing through pins (5), (6) and (7) of IC403, enters pin (5) of IC401. Also the signal out of pins (5), (6) and (7) of IC403, passing through Q415, enters pin (6) of IC401. The input at pin (6) of IC401, forming the high-pass filter, is subjected to the limiter inside the IC, where noise components are eliminated. The signal fed to pin (5) of IC401 has the noise removed and is fed out of pin (6), which completes noise cancellation. The noise-cancelled signal enters the 75-ohm driver line of the Y/C mixing amplifier, and the Y/C-mixed signal through pins (32), (33) and (34) of IC401 is fed out of pin (36) of IC401. (The same path as the camera EE Y signal).

(6) Flow of playback C signal

The mixed FM wave (PB-C RF) out of the head amplifier is provided with the ATF trap (150 kHz) and AFM trap (1.5 MHz) before Q3403, and is fed to pin (45) of IC401.

The input signal, passing through the PB C low-pass filter, is deprived of signals except the low-frequency chroma components, and fed to the ACC circuit. Here absorbed are the level fluctuations due to the head level difference and that in the low-frequency chroma signal.

The low-frequency chroma signal with restricted level fluctuations is inputted to the playback converter circuit, and returned to the carrier chrominance signal in a procedure opposite to the recording. (732.42 kHz → 4.433619 MHz). At this time, PS processing is also performed to provide the phase of the original signal. The carrier chrominance signal, which has been returned from the playback converter circuit and contains a sum component due to balanced modulation, is fed through the band-pass filter. The color signal in this condition contains much crosstalk of adjacent tracks. Therefore the chroma components of adjacent tracks are separated by means of the comb filter used for Y/C separation in recording, in order to suppress the chroma crosstalk. The comb filter in playback returns the crosstalk components to the input by negative feedback, thereby improving picture quality. (The flow of signals in the delay line is the same as that in the Y/C separation.)

The signal deprived of crosstalk passes through the band-pass filter, where the signal emphasized in recording in the burst deemphasis and chroma deemphasis circuits is returned to the original condition. The chroma signal thus obtained is fed out of pin (63) of IC401. At this time, if no color signal is recorded, the ACK operates and pin (63) of IC401 becomes low in level.

The color signal out of pin (63) of IC401 is fed to pin (2) of IC2401 for compensation of decolorization in special playback. In this IC, decolorization in the search mode or the still mode is turned into pseudo burst for correction. The normal playback signal is outputted by "through". The signal coming out of pin (15) of IC2401, passing through Q433, is fed to pin (64) of IC401 and fed to the Y/C mixing amplifier's 75-ohm driver line, and the Y/C-mixed signal is fed out of pin (36) of IC401. (The same as the camera EE C signal).

(7) Flow of LC video output

1) Camera output/playback output

The camera and playback signals are taken out in the halfway along the Y/C mixing amplifier's 75-ohm driver line of IC401 as a Y/C-separated signal, and the resulting signal Y/C-mixed in IC1401 (NJM2509V) (where 6-dB amplification is performed to provide 1 Vp-p). The signal is supplied to the LCD circuit.

The camera/playback Y signal fed to pin (32) of IC401 and the camera/playback C signal fed to pin (64) of IC401 are branched off and go to pins (1) (Y input) and (3) (C input) of IC1401 respectively.

Here the signal is Y/C-mixed and fed out of pin (8) of IC1401. The signal is further fed to pin (8) of IC1402, and out of pin (6), and supplied to the LCD circuit. Operation of the IC1402 will be discussed after.

2) Flow of external input(VL-E30X, E40X, E7E/D, E8E/D)

The externally inputted signal is a Y/C-mixed signal. The signal fed to pin (32) of IC401 is branched and fed to pin (1) of IC1401. At this time, Q433 stays off so that no noise is mixed at pin (3) of IC1401. The path thereafter is the same as in the above step 1).

3) Monitor input (video printer signal input)

The monitor input terminal of the AV box is an input terminal for monitoring the picture when the video printer is in use.

The signal outputted from the AV box is fed to the video printer and the signal outputted from the video printer is returned to the AV box monitoring input terminal, which enables monitoring of printed pictures. By inserting a pin jack into the AV box monitor input terminal, a switching signal for the LC display signal is produced, and the video printer signal is fed to pin (6) of SC601, while and the switching signal to pin (5). At this time, the video printer signal is terminated with 75 ohms inside the AV box and provided with 1 Vp-p.

The printer signal is fed to pin (9) of IC1402, and the switching signal Hi to pin (7) of IC1402. The switching signal changes the output from pin (6) of IC1402 from the video output signal to the printer input signal, and the signal is supplied to the LCD circuit.

15. Y/C SIGNAL PROCESSING CIRCUIT (NTSC)

* Refer to the VL-MX series manual for details of the 8mm video standard.

<Video Circuit (NTSC) of Models VL-E30U/C, E35U/E35, E40U/C>

A single-chip Y/C circuit CXA1700R is employed for the E30/E40 series models. Its major functions and the signal flows in the video system are discussed below.

15-1. Functions of the main signal processing IC (IC401: CXA1700R)

(1)	Input/output functions	Switching of input signal for two lines
		Video AGC
		Sync separation
		Y/C mixing, 75-ohm video output driver
		Y/C separation comb filter
		Y signal H correlation detection
(2)	Y line functions	Y preemphasis/deemphasis
		White/dark clip
		Clip compensation
		HHS/HHS cancellation
		Y FM modulation/demodulation
		Y dropout compensation
		Y/C crosstalk removal
(3)	C line functions	ACC
		C emphasis/deemphasis
		Burst emphasis/deemphasis
		XO/VXO
		APC/AFC
		APC ID/AFC ID/Burst ID
		ACK
		APC correction
		HHK
		PI/PS
		Frequency conversion system
		PB C BPF/REC C LPF
		PB C LPF/Carrier BPF

* Switching and characteristics change in the IC are controlled by serial data (32 bits).

15-2. Signal Processing Paths

(1) Flow of camera EE signal

The Y signal output from the camera PWB (CAM Y) is supplied to pin (11) of connector SC702 of the VCR PWB, and then to pin (11) of IC1402 (NJM2285M). Here the recording characters, such as date and time, are combined with the border lines of the characters and fed out of pin (5).

The CAM Y signal is inputted to pin (30) of IC401 (CXA1700R) and fed to the 75-ohm driver line of the Y/C mixing amplifier when the video AGC is turned off (serial data 29 bits: L). The path is the line from the output pin (34) of IC401 to the input pin (32) of IC401.

On the other hand, the C (CAM C) signal going from the camera PWB is supplied to pin (13) of connector SC702 (VCR PWB) and fed to pin (16) of IC1402. Here the chroma signal is muted only in the range containing characters so that no color component is mixed with the recording characters.

The CAM C output from pin (3) of IC1402 is fed to pin (53) of IC401 for dot correction, then goes to the 1H CCD line input line and goes out of pin (23) of IC401. When only the chroma signal is fed to IC402 (CXA5502N) (IC402 used in the bias mode), the maximum input amplitude is limited to a half compared to the input of Y/C mixing signal (IC402 used in the clamp mode).
Therefore the signal is attenuated by 6 dB at the input of Q1403, and distributed between the main signal and the delay signal at the output of Q1403.
The main signal, passing through Q1403 and Q1405, is mixed with a signal 1H behind at Q1406, and the dot-corrected signal is fed out of pin (2) of Q1406. ("dot" refers to a pseudo signal which appears in a luminance signal when a color signal has no vertical correlation. In order to suppress the dot disturbance, the signal is mixed here with a signal 1H behind to equalize the chroma signal, reducing the level of the pseudo signal appearing in the Y signal.) The dot-corrected CAM C signal, passing through Q433, is fed to pin (64) of IC401 and enters the 75-ohm driver line of the Y/C mixing amplifier.
The resulting signal is fed out of pin (36) of IC401 and supplied to the AV box via pin (4) of SC601.

(2) Flow of camera record Y signal

The camera record Y signal is carried to pin (30) of IC401 along the same path as the camera EE (Y) signal and branched into the EE path and the record path inthe IC.
The signal, passing through the video AGC in the off mode, is fed to the equalizer block (fsc trap and Y low-pass filter) and out of pin (14) of IC401. The output signal from pin (14) of IC401 is further fed to the equalizer Q409 of the external circuit, and is corrected in phase generated in the IC. It passes through Q412 and enters pin (5) of IC401 with the level of emphasis input which has been adjusted at pins (5), (6) and (7) of IC403 (BA7655AF).
The input signal from pin (5) of IC401, passing through the preemphasis circuit composed of the main emphasis and subemphasis, is white/dark-clipped (preset value: white clip 220% and dark clip 100%). The emphasis circuit refers to a circuit to emphasize the high-frequency band, and the high-frequency band is attenuated (deemphasized) in playback, thereby improving the signal-to-noise ratio without degrading the details information. As for clipping, the spike generated in the emphasis is cut at a specified level (controlling an over-modulation in the FM circuit) to suppress the inversion phenomenon in playback.
The clipped signal, further passing through the smear correction circuit, is subjected to carrier adjustment (sync tip: 4.2 MHz) and deviation adjustment (between the sync tip and white peak: 1.2 MHz). Then it passes through the HHS (Half H Shift) circuit where the FM frequency of the odd-numbered field's signal is carrier-shifted by 1/2H in order to reduce the crosstalk of adjacent tracks.
Thus the FM-modulated signal is fed out of pin (39) of IC401.
The Y-FM signal, passing through Q3404, has the side band component near 743 kHz/1.5 MHz removed by the low-frequency chroma trap and AFM trap, and is fed through the equalizer (Q3405) to correct the FM waveform distortion and sent out to the head amplifier with the recording current optimized at pins (5), (6) and (7) of IC3401 (BA7655AF).

(3) Flow of camera record C signal

The camera record C signal, is carried to pin (53) of IC401 along the same path as the camera EE (C) signal. In camera recording, the interior of the IC is in the S-REC mode (serial data 31 bits: H) and C-SEL normal mode (serial data 8 bits: L); therefore the C signal, after passing through the chroma band-pass filter, enters the ACC amplifier. This signal, of which the burst level is fixed by the ACC amplifier, is subjected to chroma emphasis (side band emphasis) and burst emphasis (burst up 6 dB) proper to the 8mm VCRs, and converted to low-frequency band (3.579545 MHz to 743.44 kHz). The 8mm VCR uses a multiple-frequency recording system, and the low-frequency conversion chroma side band is easily affected by the pilot signal and the audio signal. To cope with this, in recording, the side band is emphasized around 3.579545 MHz in modulation, and then attenuated after demodulation in playback to recover its original condition. Chroma emphasis thus contributes to an improvement in signal-to-noise ratio as the Y emphasis does.

PI (Phase Invert) processing is applied for reducing the crosstalk from adjacent tracks in low-frequency band conversion. In this process, the phase of a color signal after low-frequency band conversion is reversed every 1 H on an every other recording track in recording.

In playback, the phase is returned to the original and combined with the playback signal 1H behind. As a result, necessary signal is enlarged through synthesization with the noise-to-signal ratio improved, and unnecessary crosstalk is canceled. The chroma signal converted to the low-frequency band enters the block of record C low-pass filter, where the sum components in balanced modulation and noise components in the audio band are removed. (When a signal without burst is inputted, it is muted by the following ACK switch.)

The low-frequency band conversion chroma signal passing the low-pass filter is outputted from pin (8) of IC401 and sent out to the head amplifier with the recording current optimized at pins (1), (2) and (3) of IC3401.

(4) Flow of composite record signal (external input)

The externally inputted signal is supplied from the AV box to pin (4) of SC601 on the main PWB, terminated at a 75-ohm impedance, then fed to pin (28) of IC401. The input signal flows on when the video AGC is turned on (serial data 29 bits: H) and the S-REC mode is turned off (serial data 31 bits: H), and the signal 1H behind is added or subtracted inside the IC, and the Y/C signal is separated.

The signal in the 1H delay line is fed out of pin (23) of IC401 as a delay line signal, and goes to pin (1) of IC402 (1H CCD) via the buffer Q1403.

The 1H-delayed signal is fed out of pin (4) of IC402 (1H CCD), and enters FL401 via the buffer Q403 so that the noise above the secondary harmonic components is reduced the. The delayed signal with the noise reduced is matched in phase with the signal 1H behind in Q404, and amplified in Q405, by which the input level at pin (21) of IC401 is brought up to the specified value. Inside the IC, it is subjected to gain adjustment with the main signal, and Y/C separation is performed. The Y signal which is Y/C-separated passes through the equalizer and adds the fsc trap to the chroma component separated in order to supplement the $f_H/2$ component of the Y signal removed by the comb filter. It is mixed with the Y signal. The Y signal proceeds along the same path as the camera record (Y) signal and is fed to the equalizer block (fsc trap and Y low-pass filter). The C signal is completed when the gain adjustment of Y/C separation is finished, and proceeds to the chroma band-pass filter by the same path as the camera record (C) signal.

(5) Flow of playback C signal

The mixed FM wave (PB-Y RF), passing the RF AGC block from the head amplifier, is provided with the AFM trap (1.5 MHz), chroma trap (743 kHz), and secondary harmonic trap around Q3401 and is deprived of components other than the Y component. Further the PB-Y FM signal is inputted to the soft limiter circuit Q3402 and corrected in harmonic characteristics. This circuit serves to correct the balance of the lower wave and upper wave of the Y FM signal, thus preventing the inversion phenomenon.

The signal coming out of Q3402 is inputted to pin (41) of IC401, of which the FM level is adjusted by the limiter. Then the demodulated signal passes through the low-pass filter and is outputted from pin (7).

The signal coming out of pin (7) is shaped in the waveform by the equalizer consisting of Q417 and Q416 and by the peaking amplifier, and inputted to pin (1) of IC403.

The signal out of pin (3) of IC403 is fed to pin (10) of IC401 via Q435, and is adjusted in IC403, so that TP405 (Video OUT) has 2.0 Vp-p (alignment tape playback). This is because the video output level of the playback Y signal is determined by the input level at pin (10) of IC401.

The signal thus coming into pin (10) of IC401 is subjected to deemphasis (high-frequency attenuation circuit) and HHS cancellation (Half H Shift Cancel), and flows to the crosstalk removing circuit and the dropout correction circuit. The deemphasis circuit feeds back the signal emphasized in the high-frequency band in the emphasis circuit in recording to its original condition, and the HHS cancellation circuit returns the DC level difference in every field due to the carrier shifting recording to its original condition.

The correction signal of crosstalk/dropout, branched off the main signal, is mixed with the chroma signal and fed to the 1H/2H delay line, and finally goes out of pin (23) of IC401. (The chroma signal also enters the delay line for removal of crosstalk of adjacent tracks.)

The correction signal flows along the same path as the Y/C separation and returns to pin (19) of IC401.

The correction signal has its chroma component removed by the fsc trap in the IC, becomes a Y signal 1H delayed, and is subtracted from the signal 1H behind (Y signal branched from the main signal), thereby the crosstalk component being extracted. The crosstalk component is attenuated and then subtracted from the main signal, by which the crosstalk is removed. Further the Y signal 1H behind returning from the delay line substitutes the main signal in dropout, thereby compensating missing signals.

The Y signal with the crosstalk removed, passing through the equalizer block (sharpness correction, fsc trap), is fed out of pin (14) of IC401. The output signal passes through Q409 (equalizer) and Q412 (peaking amplifier). The peaking amplifier raises the high-frequency band in playback to improve the sharpness of the images.

The signal out of Q412, passing through pins (5), (6) and (7) of IC403, enters pin (5) of IC401. Also the signal out of pins (5), (6) and (7) of IC403, passing through Q415, enters pin (6) of IC401. The input at pin (6) of IC401, forming the high-pass filter, is subjected to the limiter inside the IC, where noise components are eliminated. The signal fed to pin (5) of IC401 has the noise removed and is fed out of pin (6), which completes noise cancellation. The noise-cancelled signal enters the 75-ohm driver line of the Y/C mixing amplifier, and the Y/C-mixed signal through pins (32), (33) and (34) of IC401 is fed out of pin (36) of IC401. (The same path as the camera EE Y signal).

(6) Flow of playback C signal

The mixed FM wave (PB-C RF) out of the head amplifier is provided with the ATF trap (150 kHz) and AFM trap (1.5 MHz) before Q3403, and is fed to pin (45) of IC401.

The input signal, passing through the PB C low-pass filter, is deprived of signals except the low-frequency chroma components, and fed to the ACC circuit. Here absorbed are the level fluctuations due to the head level difference and that in the low-frequency chroma signal.

The low-frequency chroma signal with restricted level fluctuations is inputted to the playback converter circuit, and returned to the carrier chrominance signal in a procedure opposite to the recording. (743.44 kHz → 3.579545 MHz). At this time, PI processing is also performed to provide the phase of the original signal. The carrier chrominance signal, which has been returned from the playback converter circuit and contains a sum component due to balanced modulation, is fed through the band-pass filter. The color signal in this condition contains much crosstalk of adjacent tracks. Therefore the chroma components of adjacent tracks are separated by means of the comb filter used for Y/C separation in recording, in order to suppress the chroma crosstalk. The comb filter in playback returns the crosstalk components to the input by negative feedback, thereby improving picture quality. (The flow of signals in the delay line is the same as that in the Y/C separation.)

The signal deprived of crosstalk passes through the band-pass filter, where the signal emphasized in recording in the burst deemphasis and chroma deemphasis circuits is returned to the original condition.

The chroma signal thus obtained is fed out of pin (63) of IC401. At this time, if no color signal is recorded, the ACK operates and pin (63) of IC401 becomes low in level.

The color signal out of pin (63) of IC401, passing through Q433, is fed to pin (64) of IC401 and fed to the 75-ohm driver line of the Y/C mixing amplifier. The Y/C-mixed signal is then fed out of pin (36) of IC401. (The same path as the camera EE C signal)

(7) Flow of LC video output

1) Camera output/playback output

The camera and playback signals are taken out in the halfway along the Y/C mixing amplifier's 75-ohm driver line of IC401 as a Y/C-separated signal, and the resulting signal Y/C-mixed in IC1401 (NJM2509V) (where 6-dB amplification is performed to provide 1 Vp-p). The signal is supplied to the LCD circuit.

The camera/playback Y signal fed to pin (32) of IC401 and the camera/playback C signal fed to pin (64) of IC401 are branched off and go to pins (1) (Y input) and (3) (C input) of IC1401 respectively.

Here the signal is Y/C-mixed and fed out of pin (8) of IC1401. The signal is further fed to pin (8) of IC1402, and out of pin (6), and supplied to the LCD circuit. Operation of the IC1402 will be discussed after.

2) Flow of external input

The externally inputted signal is a Y/C-mixed signal. The signal fed to pin (32) of IC401 is branched and fed to pin (1) of IC1401. At this time, Q433 stays off so that no noise is mixed at pin (3) of IC1401. The path thereafter is the same as in the above step 1).

3) Monitor input (video printer signal input)

The monitor input terminal of the AV box is an input terminal for monitoring the picture when the video printer is in use.

The signal outputted from the AV box is fed to the video printer and the signal outputted from the video printer is returned to the AV box monitoring input terminal, which enables monitoring of printed pictures. By inserting a pin jack into the AV box monitor input terminal, a switching signal for the LC display signal is produced, and the video printer signal is fed to pin (6) of SC601, while and the switching signal to pin (5). At this time, the video printer signal is terminated with 75 ohms inside the AV box and provided with 1 Vp-p.

The printer signal is fed to pin (9) of IC1402, and the switching signal Hi to pin (7) of IC1402. The switching signal changes the output from pin (6) of IC1402 from the video output signal to the printer input signal, and the signal is supplied to the LCD circuit.

16. VIDEO HEAD/HEAD AMPLIFIER CIRCUIT (PAL)

<VL-E30/E40 Series (PAL) Video Head/Head Amplifier Circuit>

The E30/E40 series video head system employs Mechanism A and consists of a drum unit of large diameter 40 mm composed of a plane rotary transformer equipped with two video heads and one erase head.

The video heads use TSS (Tilted Sendust Sputtered) head which is a type of metal head, and the erase head uses MIG (Metal In Gap) metal head in recording/playback and erasing, by winding a tape 230 degrees around the large-size drum.

The head amplifier circuit consists of a head amplifier IC (CXA1202R) and a rotary erase oscillation circuit. The function and the flow of signals are shown below:

Recording system: 2-channel recording amplifier

4-input (REC-Y, REC-C, AFM and ATF) mixing amplifier

Playback system: 2-channel head amplifier, middle frequency correction, RF AGC, dropout detection.

16-1. Flow of recording system signal

The record signals (REC-Y, REC-C, REC-AFM and REC-PILOT) out of their respective signal processing circuits are fed to pins (6), (2), (4) and (46) of IC301 (CXA1202R), respectively.

The input signal is first mixed with the chroma, audio and pilot signals which are low-frequency components, then with the Y signal. The output from pins (24) sand (37) of the mixing amplifier is converted into current by an externally added resistor, and fed to pins (25) and (36). The recording current coming out of pins (28) and (33) is driven by the recording amplifier.

The recording amplifier also applies feedback damping in order to suppress the resonance of the head. The recoding current is not switched over for every channel, so that it always flows in the two video heads.

As for the erase current, Q1304 is turned on by the "ROT ERASE" signal coming from the microprocessor, and the erasing current oscillating at approximately 8 MHz flows out of Q1301.

The erase head with two tracks of head width traces the track prior to the head of channel 1 and channel 2 as erasing the tape, in the same way as on conventional models.

16-2. Flow of playback system signal

The playback signals out of CH-1 (microprocessor control signal "H-SW-P" at high side, playback video signal at field 1 side) and CH-2 (microprocessor control signal "H-SW-P" at low side, playback video signal at field 2 side) are fed to pins (29) and (32) respectively, then amplified by the head amplifier having a gain of approximately 55dB, and fed to the middle frequency correction circuit.

In the middle frequency correction circuit, the output balance of the head amplifier (frequency characteristics) is corrected to prevent the inversion phenomenon in the video system. The center frequency and Q are set in the external resistors at pins (26) and (35), and the boost amount is determined by the DC voltage applied at pins (23) and (38).

The output from the middle frequency correction circuit activates the video switch inside the IC through the H-SW-P signal, and becomes a continuous wave to be outputted from pins (10) and (20).

The output signal from pin (20) is amplified by 12 dB by Q302 and supplied via the buffer to the Y/C circuit (chroma signal processing system), audio circuit and servo circuit.

The signal fed out of pin (10), being sent through the RF AGC circuit, is detected in the band of the FM Y signal, and the signal of 100 mVp-p is outputted. Further, the signal passing through the AGC is inputted to pin (14), amplified by the 12-dB amplifier inside the IC, and fed out of pin (16).

The signal fed out of pin (16) is supplied to the Y/C circuit (Y signal processing system) via the buffer, as well as fed to pin (18), where the dropout is detected. The dropout pulse is fed out of pin (13) at "High" at the time of dropout.

16. VIDEO HEAD/HEAD AMPLIFIER CIRCUIT (NTSC)

<VL-E30/E40 Series (NTSC) Video Head/Head Amplifier Circuit>

The E30/E40 series video head system employs Mechanism A and consists of a drum unit of large diameter 40 mm composed of a plane rotary transformer equipped with two video heads and one erase head.
The video heads and the erase head use MIG (Metal In Gap) metal heads, and record/playback as well as erase are performed by winding a tape 230 degrees around the larger drum.

The head amplifier circuit consists of a head amplifier IC (CXA1202R) and a rotary erase oscillation circuit. The function and the flow of signals are shown below:

Recording system: 2-channel recording amplifier
4-input (REC-Y, REC-C, AFM and ATF)mixing amplifier
Playback system: 2-channel head amplifier, middle frequency correction, RF AGC, dropout detection.

16-1. Flow of recording system signal

The record signals (REC-Y, REC-C, REC-AFM and REC-PILOT) out of their respective signal processing circuits are fed to pins (6), (2), (4) and (46) of IC301 (CXA1202R), respectively.
The input signal is first mixed with the chroma, audio and pilot signals which are low-frequency components, then with the Y signal. The output from pins (24) sand (37) of the mixing amplifier is converted into current by an externally added resistor, and fed to pins (25) and (36). The recording current coming out of pins (28) and (33) is driven by the recording amplifier.
The recording amplifier also applies feedback damping in order to suppress the resonance of the head. The recoding current is not switched over for every channel, so that it always flows in the two video heads.
As for the erase current, Q1304 is turned on by the "ROT ERASE" signal coming from the microprocessor, and the erasing current oscillating at approximately 8 MHz flows out of Q1301.
The erase head with two tracks of head width traces the track prior to the head of channel 1 and channel 2 as erasing the tape, in the same way as on conventional models.

16-2. Flow of playback system signal

The playback signals out of CH-1 (microprocessor control signal "H-SW-P" at high side, playback video signal at field 1 side) and CH-2 (microprocessor control signal "H-SW-P" at low side, playback video signal at field 2 side) are fed to pins (29) and (32) respectively, then amplified by the head amplifier having a gain of approximately 55dB, and fed to the middle frequency correction circuit.
In the middle frequency correction circuit, the output balance of the head amplifier (frequency characteristics) is corrected to prevent the inversion phenomenon in the video system. The center frequency and Q are set in the external resistors at pins (26) and (35), and the boost amount is determined by the DC voltage applied at pins (23) and (38).
The output from the middle frequency correction circuit activates the video switch inside the IC through the H-SW-P signal, and becomes a continuous wave to be outputted from pins (10) and (20).
The output signal from pin (20) is amplified by 12 dB by Q302 and supplied via the buffer to the Y/C circuit (chroma signal processing system), audio circuit and servo circuit.
The signal fed out of pin (10), being sent through the RF AGC circuit, is detected in the band of the FM Y signal, and the signal of 100 mVp-p is outputted. Further, the signal passing through the AGC is inputted to pin (14), amplified by the 12-dB amplifier inside the IC, and fed out of pin (16).
The signal fed out of pin (16) is supplied to the Y/C circuit (Y signal processing system) via the buffer, as well as fed to pin (18), where the dropout is detected. The dropout pulse is fed out of pin (13) at "High" at the time of dropout.

17. LCD CIRCUIT

17-1. OUTLINE

The LCD circuit employs a 2-chip LSI (a single-chip design of the decoder and interface as well as a TFT-LCD controller IC) for fewer peripheral parts and smaller LSI packaging. This circuit is lightweight too due to a 6-layer PWB design.

17-2. OPERATION

Below shown is the basic LCD circuitry. Referring to the block diagram, the circuit behavior is discussed block by block.

17-2-1. Decoder/interface circuit

IC800 (IR3P90Y1-NTSC, IR3Y21-PAL) is a small multi-function IC in which the NTSC, PAL color LCD viewfinder video/chroma signal processor and interface are stored in a single chip. This IC has various types of filters built-in, by which many external parts can now be eliminated. The video AGC circuit and gamma (γ) correction circuit are also incorporated as so to meet the unique characteristics of the LCD panels.

The main features are:

① 3.58-MHz (NTSC), 4.43-MHz (PAL) band-pass filter, 3.58-MHz (NTSC), 4.43MHz (PAL) trap and delay line incorporated
② APC adjustment no longer needed
③ Secondary differential picture quality adjustment circuit
④ Polarity inverter circuit
⑤ Video AGC circuit
⑥ Gamma (γ) correction circuit
⑦ Compatible with external RGB input signal

The IR3P90Y1 (NTSC), IR3Y21 (PAL) is roughly divided by function in two sections; decoder and interface.

In the decoder section, the composite video signal is fed in pin (10) of IC800. The composite signal is separated to the luminance signal and chroma signal. The luminance signal is used for AGC and picture quality correction. In the AGC circuit, different AGC characteristics are obtained due to the APL level of the luminance signal. High-frequency components are removed from the luminance signal by the filter at pin (17) and the resulting signal is peak-detected by the AGC detector. In the picture quality adjustment circuit, the luminance signal is secondary-differentiated and its high-frequency components are reduced in noise level. The then signal is gain-adjusted with the terminal voltage at pin (23), and the resulting signal is mixed with the luminance signal. By so doing, the luminance signal's frequency characteristics can be properly adjusted. The chroma signal, on the other hand, goes through the ACC detector and ACC amplifier to peak-detect the amplitude of the burst signal. This forms the ACC loop. After being demodulated, the chroma signal is converted by the matrix-circuit to the luminance signal as well as the R, G and B primary-color signals. The VCO local oscillator circuit is composed of a Pierce type quartz oscillator circuit. The APCdetector is used to phase-detect the burst signal and the VCO oscillation output. By controlling the detection voltage and the VCO oscillation frequency, the PLL loop is formed, thereby requiring no adjustment any longer.

Let us now discuss the interface section. The interface section is additionally provided with the following circuits.

① External R, G and B signal switching circuit
② R and B gain control circuit
③ Pedestal clamp circuit (brightness control)
④ Gamma (γ) correction and peak limiter circuits
⑤ Inverter circuit (polarity inversion)

- External R, G and B signal switching circuit
  The switching circuit is of analog switching type. The control signal being fed to pin (1) is used to switch between the internal primary color signal (INT) from the video/chroma circuit and the external signal (EXT) from the external R, G and B input terminals. The high-speed analog switch is set to the INT position with a low signal, and to the EXT position with a high signal or in an open state.
  This circuit serves to give on-screen color display. The digital on-screen signal is fed to the external input terminal for character display. The switching control signal feeds blanking pulses for on-screen display to pin (1). The waveform is shown in Fig. 17-1.

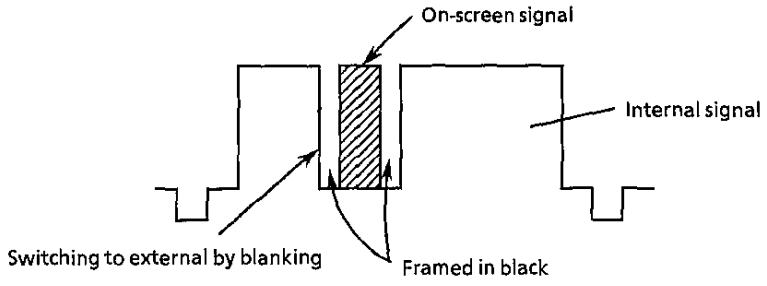
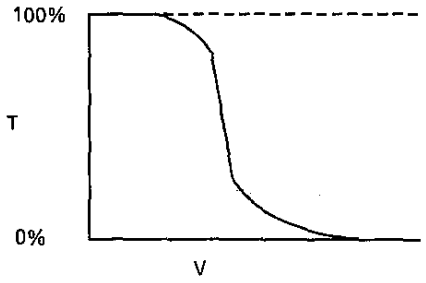


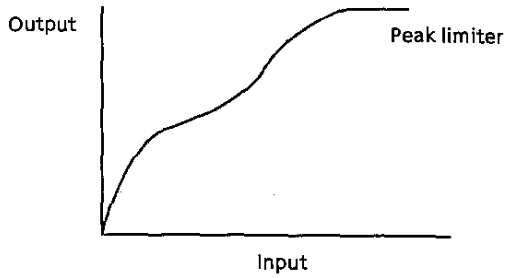
Figure 17-1.

- R and B gain control circuit
  The DC voltages being applied at pins (41) and (42) are used to gain-control the B and R signals. With the gain control, the contrast can be finely adjusted.
- Pedestal clamp circuit
  The DC voltage being applied at pin (43) is used to vary the pedestal level, by which the brightness is controlled.
- Gamma (γ) correction and peak limiter circuits
  The V-T characteristic of the LCD panels is not linear, but as shown in Fig. 17-2(a). When a linear video signal is applied to the panels, the color tones around the white peak as well as around the black pedestal are degraded and the linear brightness characteristic is not achieved. To get the proper characteristic, it is necessary to apply the video signal which corresponds to the panel's V-T characteristic.
  By applying gamma (γ) correction and peak limiter to the video signal, therefore, a dynamic, linear brightness characteristic is obtained, thereby offering a fidelity reproduction. Fig. 17-2(b) shows the gamma (γ) correction characteristic.



V-T characteristic

Figure 17-2(a).



Gamma (γ) correction

Figure 17-2(b).

- Inverter circuit (polarity inversion)

No DC voltage can be applied to the LCD panels. This means that the video signal to go to the panels must be inverted in polarity. The inverter circuit serves to invert the polarity. The FRPV pulse being fed to pin (39) makes inversion of the polarity of R, G and B primary color signals (at pins (32), (34) and (36)) every 1H.

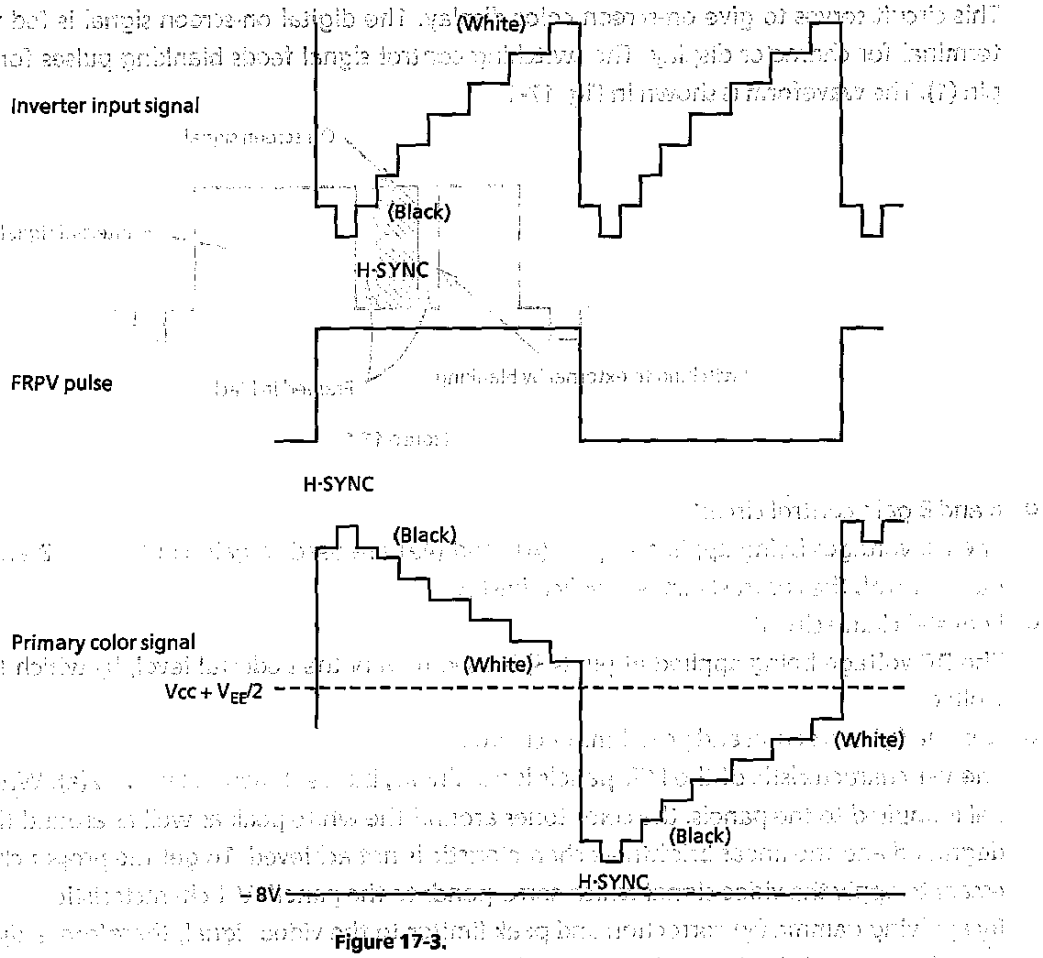


Figure 17-3.

The FRPV pulse also makes polarity inversion field by field.

This way, the DC power is converted to AC one in order to protect the LCD against deterioration. Fig. 17-3 shows the pulse timing.

The LCD panels are commonly used for both the PAL and NTSC systems.

In order to convert the PAL system signal in the NTSC signal, a skipping method is adopted. The skipping timing is as follows: one every six lines, one every eight lines (2 every 14 lines), and 44 or so lines every field.

17-2-2. TFT-LCD sync controller IC

IC801 is a TFT-LCD module sync controller IC. Fig. 17-4 shows the block diagram. This IC is a plastic flat package, measuring 10 mm by 10 mm, with 48 pins spaced in 0.75 mm pitches.

(3-inches: RH-IX0180TAZZ, 4-inches: RH-IX2089CEZZ)

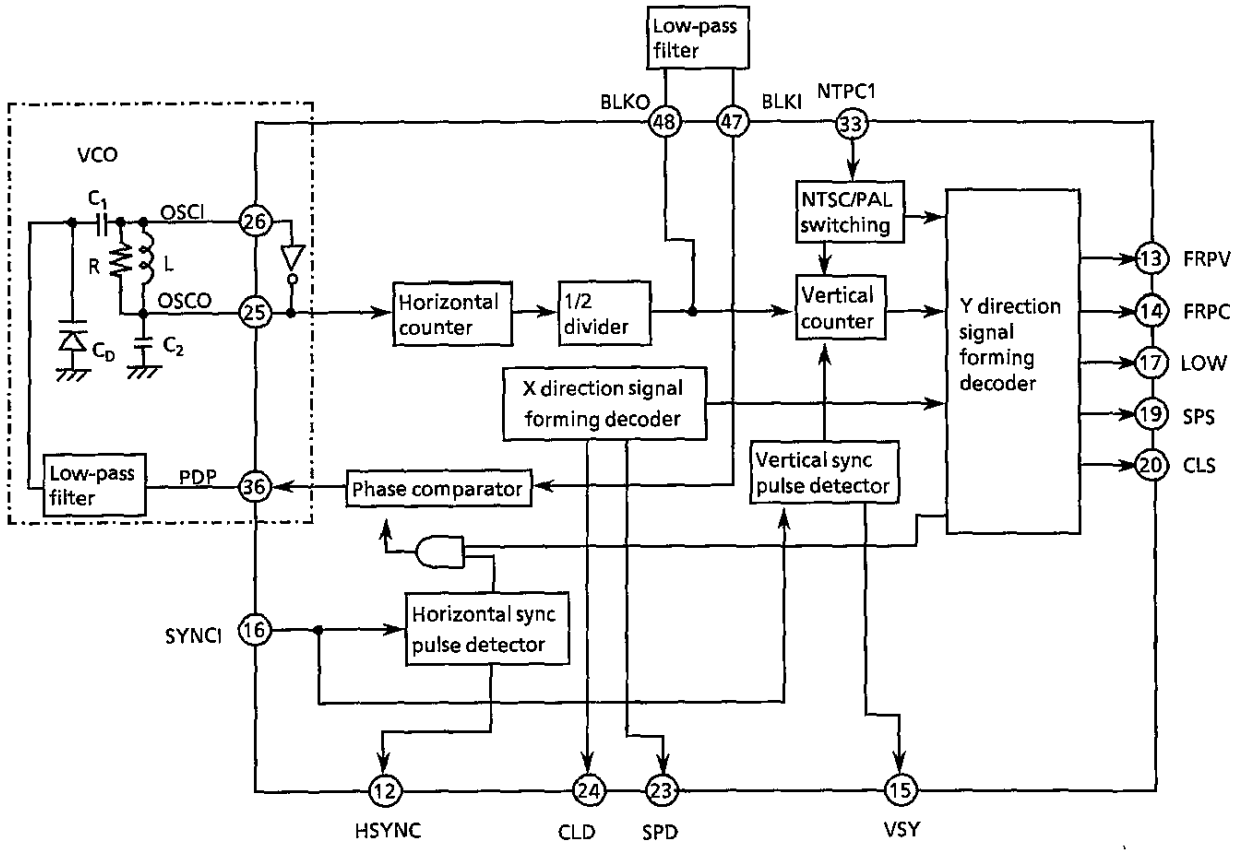


Figure 17-4.

(1) VCO circuit construction

In the VCO circuit, two pulses are compared as to their phases; one pulse is the delayed pulse (BLKI), which is produced from the output pulse (BLKO) coming from the oscillation circuit (composed of C_1, C_2, R, L and varicap diode C_D as shown in Fig. 17-4), and the other pulse is the input C sync pulse. As a result of the comparison, the PDP pulse goes out of pin (36). This pulse passes through the low-pass filter and into the oscillation circuit.

Corresponding to the applied voltage, the voltage being applied to the varicap diode is controlled to vary the capacitance (C_D). In this way, the oscillation frequency is controlled and the input C sync gets locked.

(2) PDP pulse

The PDP pulse is a phase-compared output pulse and as shown in Fig. 17-5.

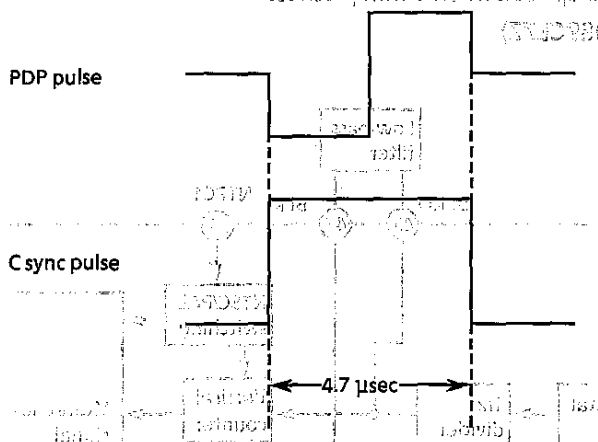
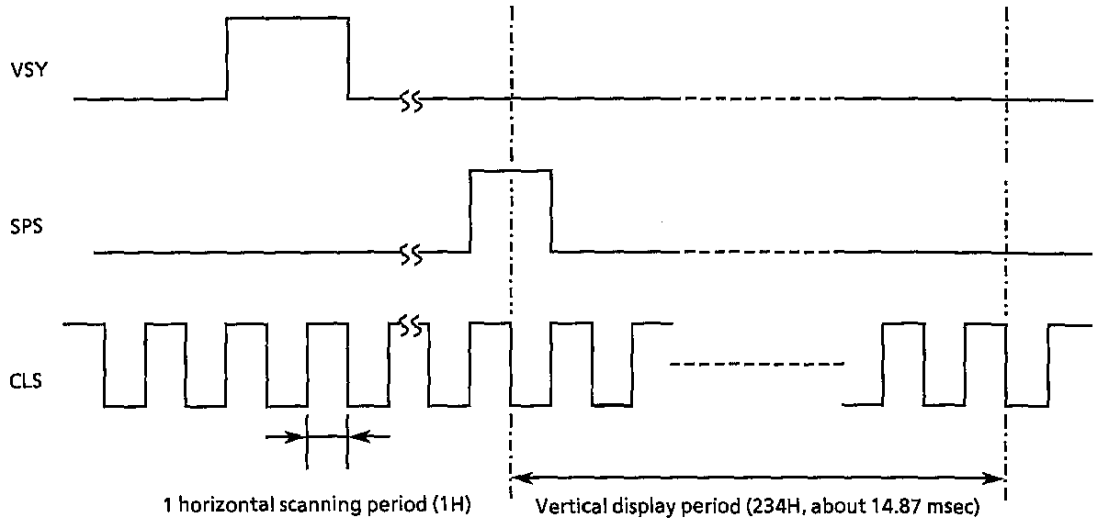


Figure 17-5.

(3) Terminals and Functions

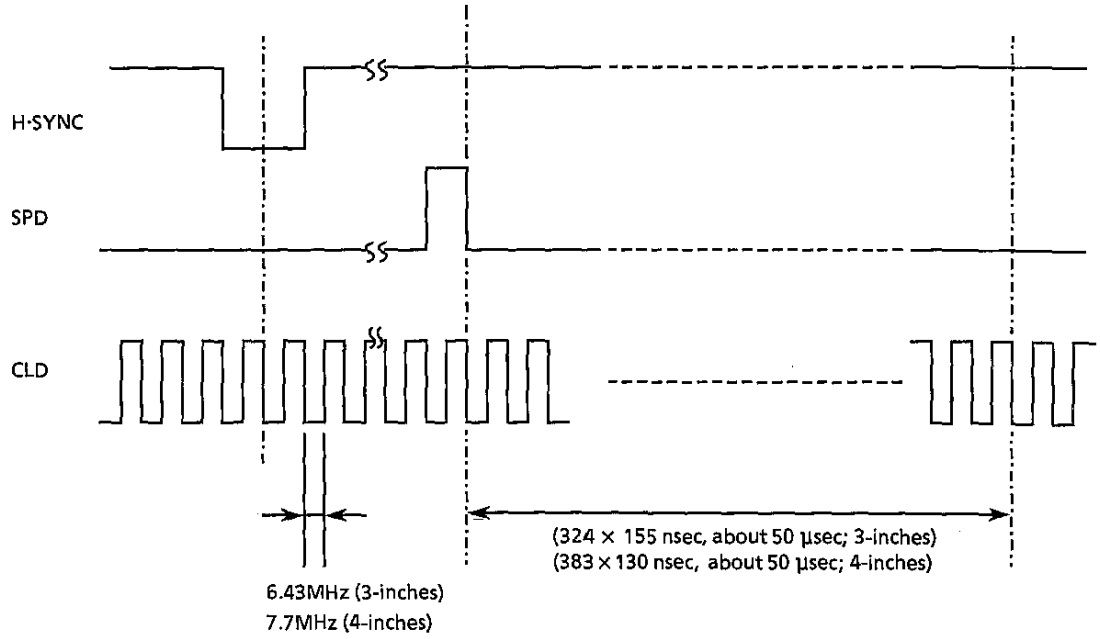
Terminal name	Function
SPS	Vertical driver start signal output
CLS	Vertical driver clock signal output
LOW	Vertical driver low signal output
SPD	Horizontal driver start signal output
CLD	Horizontal driver clock signal output
CSP1	Horizontal driver color switching signal output
FRPV	Video signal polarity inversion signal output
P15	Noiseless QVD input
P16	Noiseless W/H input
VREVC	Top/bottom reverse setting terminal
EX1	Top/bottom reverse output terminal

(4) Display period counter timing

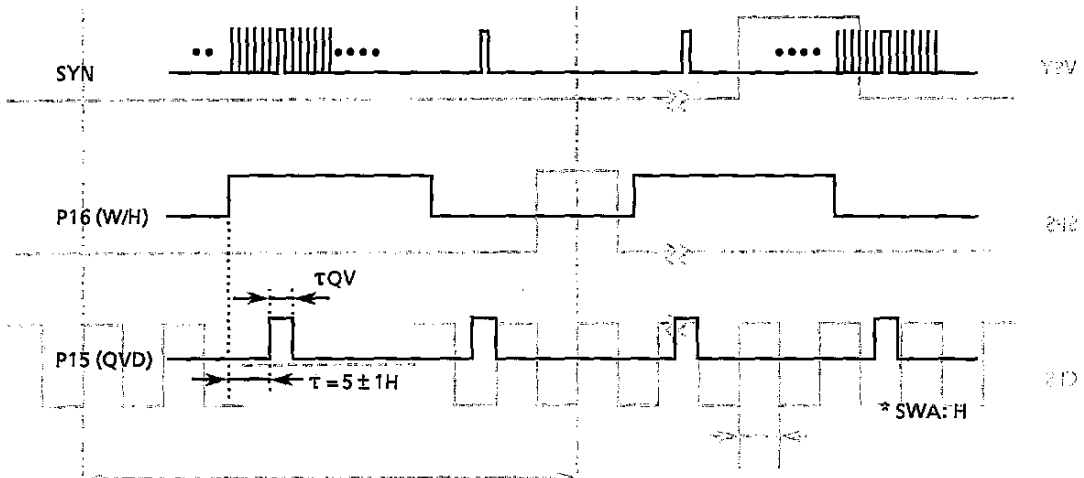


The skipping process is made for the PAL system signal. The CLS pulse is held to skip necessary lines. If the same line is skipped in the odd-numbered and even-numbered fields, one line will be missing. To avoid this, the field-to-field timing is properly shifted.

(5) Horizontal display



(6) Noiseless drive waveform



Noiseless drive terminal function: P15, P16

P16 (W/H) terminal

When the terminal gets low in level, the noiseless drive mode is brought in.

The normal mode comes back when the high-level state continues for 2 fields.

In the W/H drive mode, while the W/H terminal stays low in level, the video signal is not written on the display panel.

The input signal for the W/H terminal, therefore, must have a waveform, the level of which is inverted in the odd-numbered and even-numbered fields. The low-level signal must not be allowed continuously for longer than one-field period.

Note: Usually keep the terminal at high level or open. If used in the noiseless drive mode for a long time, the display quality may be degraded.

P15 (QVD) terminal

In the noiseless drive mode, the signal coming to this terminal becomes a vertical sync signal. Therefore, a positive-polarity vertical sync signal is needed. (The sync position is determined by the rising edge of the signal.)

② Horizontal drive (2-phase drive)

Horizontal picture elements are transferred within a single horizontal scan time. The horizontal drive frequency is determined as follows depending.

$$\text{Horizontal drive frequency} = \frac{1}{\dfrac{\text{Effective horizontal scan time *}}{\text{Electrical effective number of horizontal picture elements}}} = \frac{1}{\dfrac{51.9 \times 10^{-6}\,(\text{sec.})}{491\ (\text{Picture elements})}} \fallingdotseq 9.46\ (\text{MHz})$$

* 64.0 – 12.1 = 51.9 (μsec.)

The frequency is approx. 9.46 MHz, enabling high speed operation.
øH1 and øH2 are square waves of 50% duty with 180° phase difference from each other.
Figure 5-7 shows the horizontal transfer timing chart.

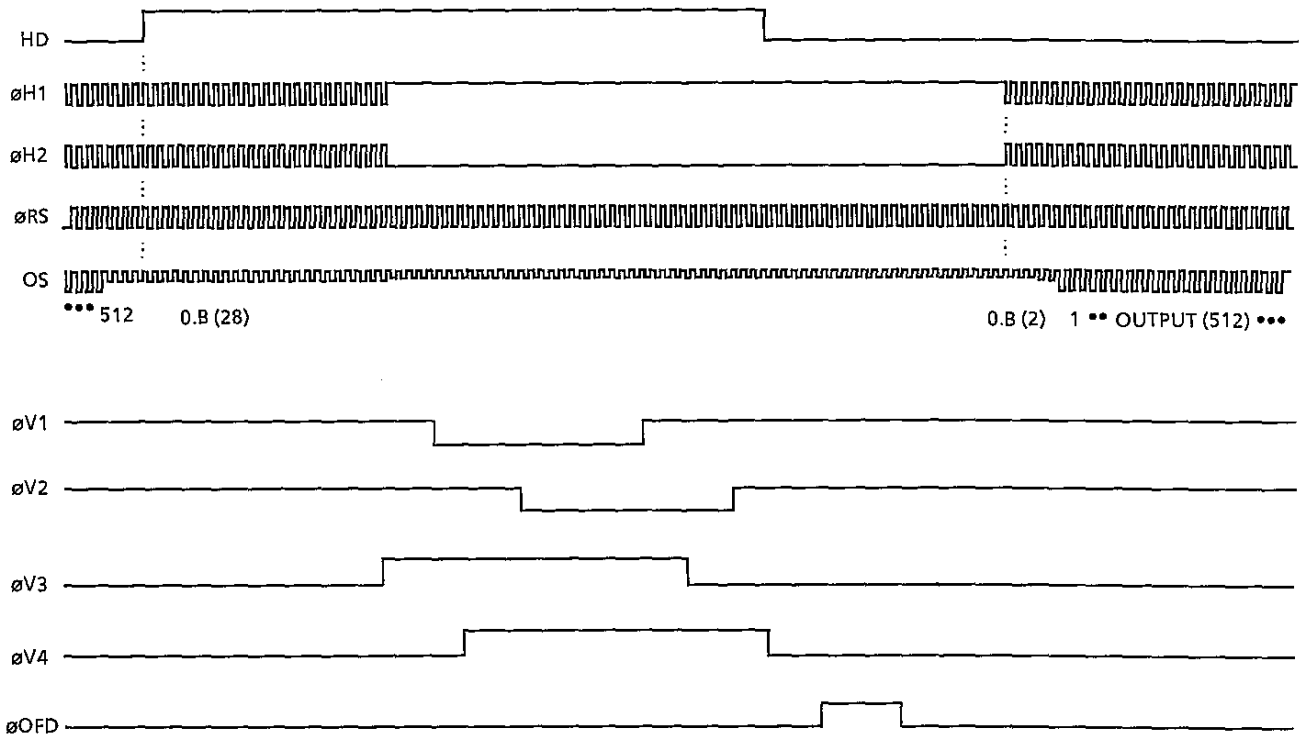


Figure 5-7. Horizontal Transfer Timing Chart

5-5. Color filter

Figure 5-8 shows the arrangement of the color filter.
Figure 5-9 is an illustration of the sensor signal read-out process.

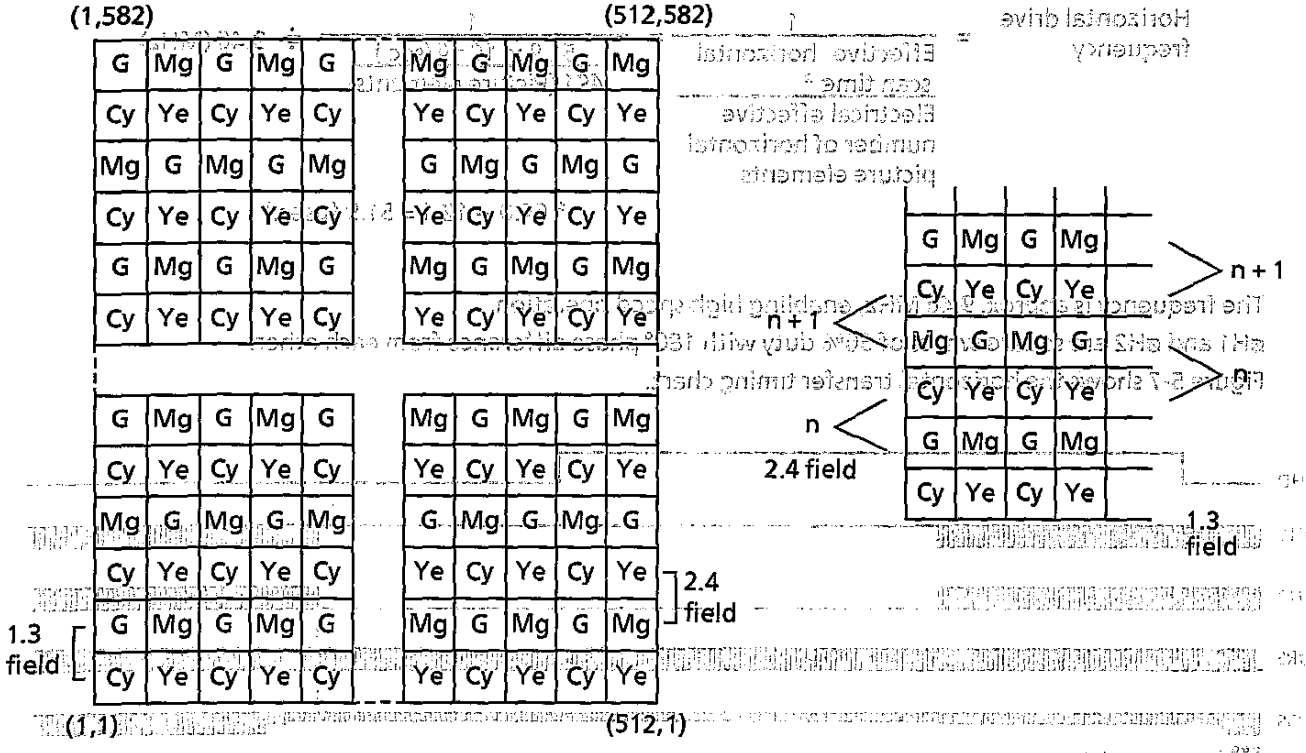


Figure 5-8. Color Filter Arrangement

Figure 5-9. Illustration of Sensor Signal Read-out Process

As shown in Figure 5-9, each field has horizontal lines of filters in common that make up the signal read-out. Therefore, the signals coming from the horizontal shift register are as follows.

1.3 field	n line	(Cy + Mg), (Ye + G), (Cy + Mg) . . . . .
	n + 1 line	(Cy + G), (Ye + Mg), (Cy + G) . . . . .
2.4 field	n line	(G + Cy), (Mg + Ye), (G + Cy) . . . . .
	n + 1 line	(Mg + Cy), (G + Ye), (Mg + Cy) . . . . .

These signals are used to make up the video signal. Explained next are the processes in which luminance signal (YH signal) and chrominance signal (color difference signals R-Y and B-Y) are produced.

5. CCD OPERATION (LZ24135) (VL-E30U/C/E35U/E35, E40U/C)

5-1. Outline and features

The cameras use a is 1/4" solid state CCD that has 270,000 picture elements (effective 250,000). Figure 5-1 shows the composition of these picture elements.

The CCD is an inter-line system with field accumulation employing a complementary mosaic color filter.

The camera is equipped with V-OFD (vertical type overflow drain) high speed shutter, which requires no memory device .

(Shutter modes: 1/60 and 1/500 (sports mode))

The major features are:

- 1/4" 542(H) × 492(V) Approx. 270,000 picture elements
  (Effective picture elements: 512(H) × 492(V) Approx. 250,000)
- Blooming suppression
- Variable electronic shutter function (2 modes in this model)

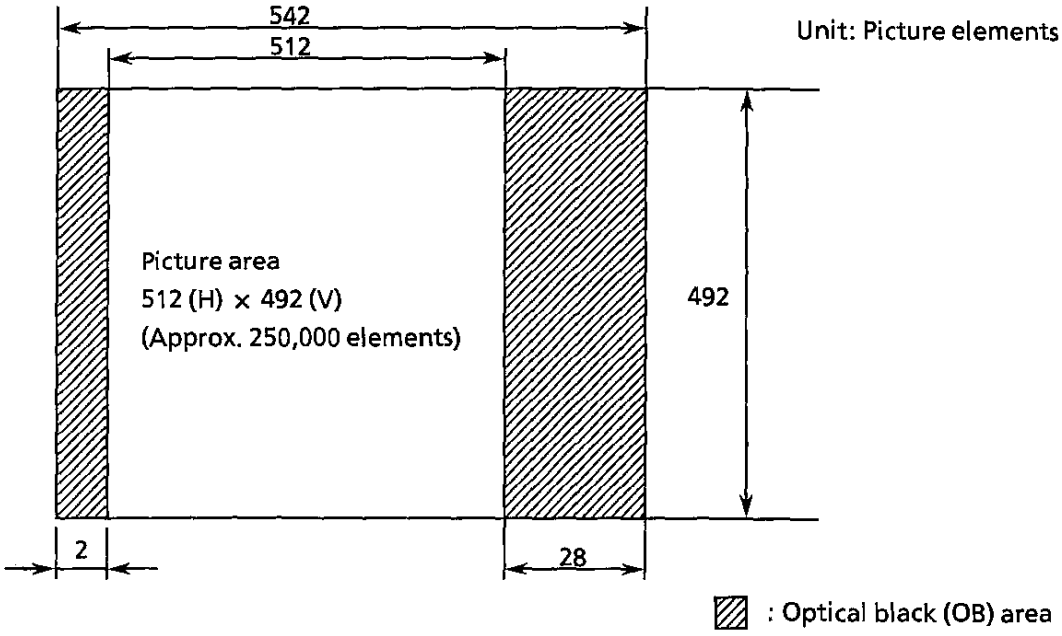


Figure 5-1. Picture Elements Composition

5-2. Basic operation of a CCD camera

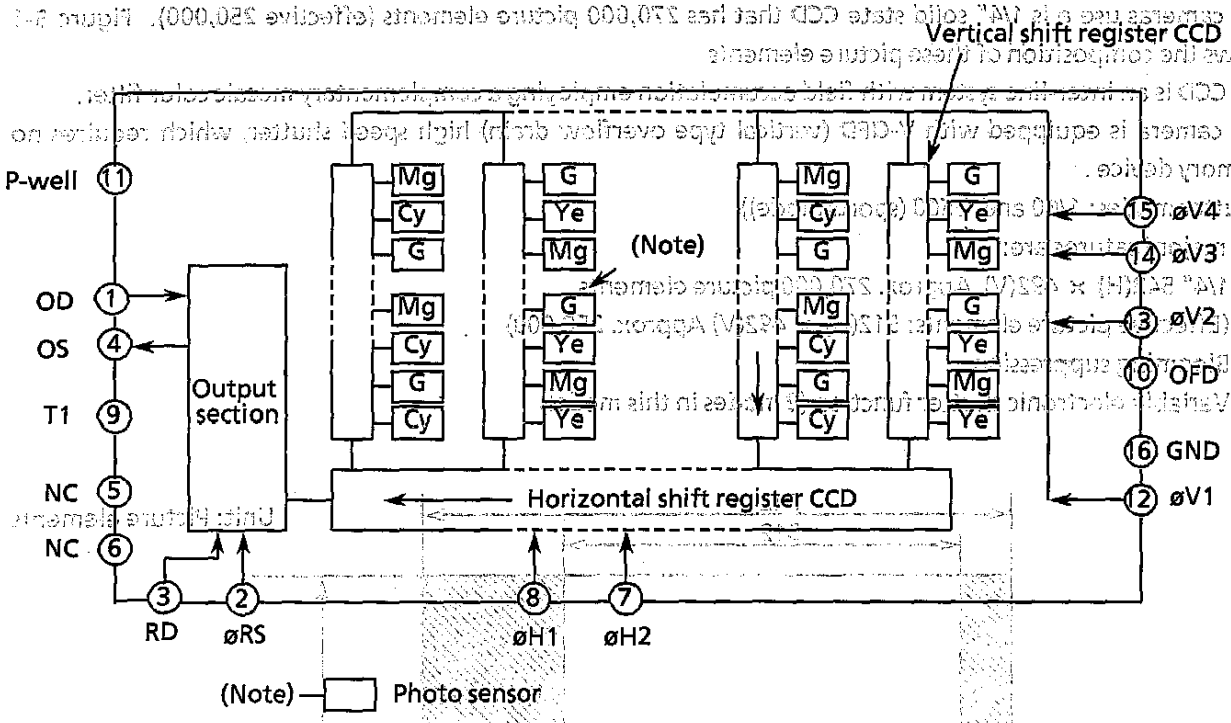


Figure 5-2. Internal Block Diagram

- Refer to Figure 5-2. When the photo sensor receives light, an electric charge corresponding to its intensity will be produced and stored.
- The charge is then sent out to the vertical shift register during the vertical blanking period by the sensor's charge read-out pulses SG1 and SG2, which are overlaid on the vertical transfer clock signals øV1 and øV3.
- The signal charge read out to the vertical shift register is transferred to the horizontal shift register by the vertical register transfer clock signals øV1 ~ øV4. This is done step by step for every horizontal blanking period.
- The signal charge transferred to the horizontal shift register is then sent to the output section by the horizontal register transfer clock signals øH1 and øH2 within the horizontal scan time (1H: 64 µsec), covering the number of horizontal elements.
- In the output section, the charge detection capacitor, which is initialized by the reset gate clock signal øRS, receives its charge from the horizontal shift register and outputs the electric potential corresponding to the charges received. This electric potential is amplified by the output amplifier to produce CCD signal .

5-3. High speed shutter operation

The CCD image sensor adopted in this model enableds the draining of unnecessary charge in every horizontal scan during the horizontal blanking period, enhancing the high speed electronic shutter operation. Thus, while having no memory section for the high speed shutter operation, various shutter modes have been made available.

① V-OFD (Vertical overflow drain)

As shown in Figure 5-3 (a), Vsub voltage is applied to the n-substrate during normal operation, suppressing the generation of excessive charge which will cause smearing or blooming.

When the electronic shutter is operated, Δ Vsub voltage is added to drain the charge accumulated in the sensor output of the substrate. (Figure 5-3 (b))

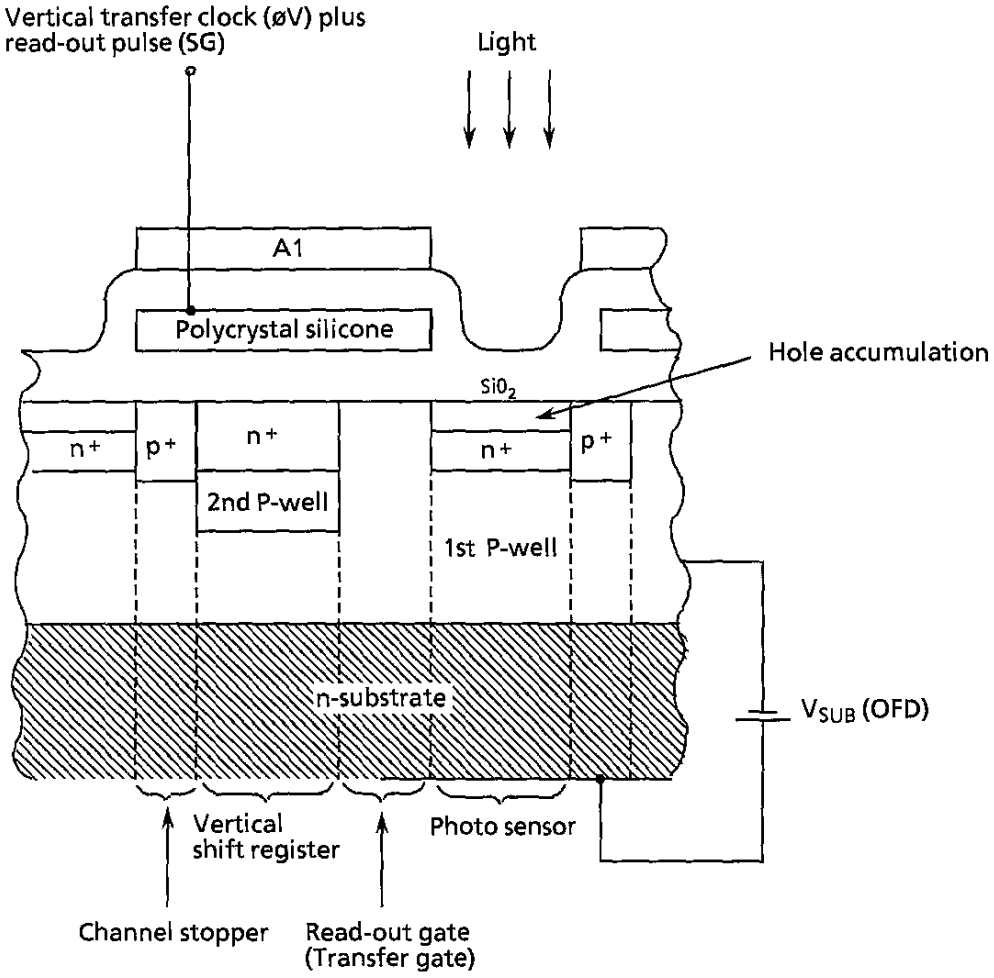


Figure 5-3 (a). Sectional View of CCD Image Sensor

Smearing: When the sensor receives intensive light, the generated charge leaks out to the vertical register. This appears as vertical white lines in the picture.

Blooming: When there is a single extremely bright spot in the picture, the charge from the photo sensor will fill up the transfer gate and the channel stopper. As a result, the light appears to surround the bright spot.

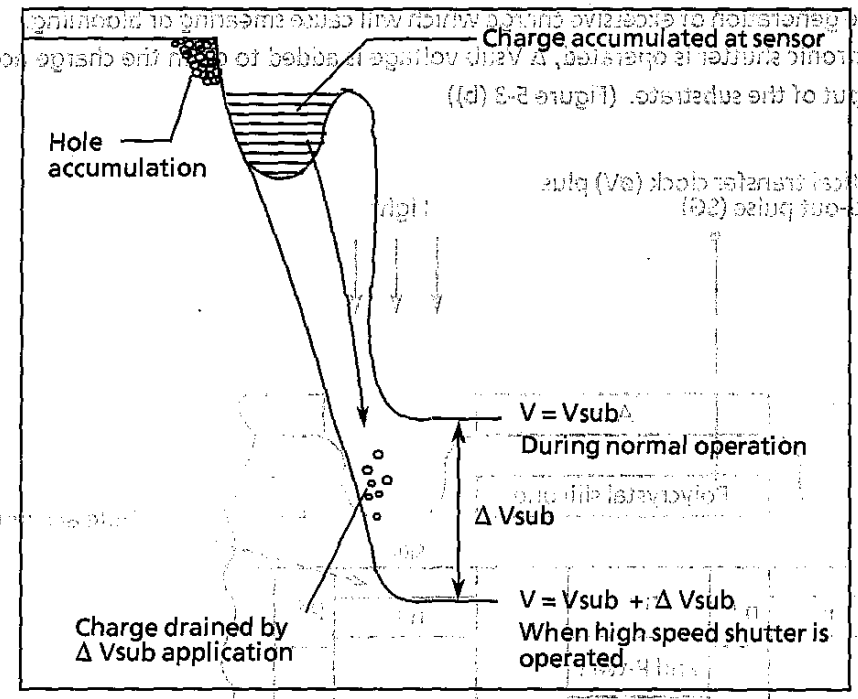


Figure 5-3 (b). Vertical Potential Distribution at Sensor Section

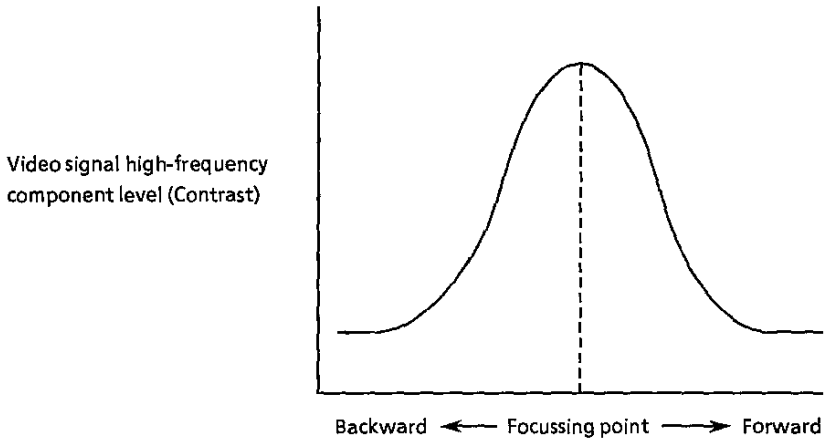


Figure 9-1. Focus lens position

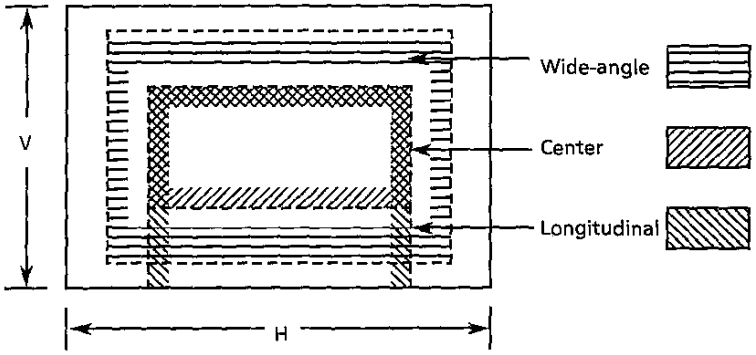


Figure 9-2. Outline of view angle gate

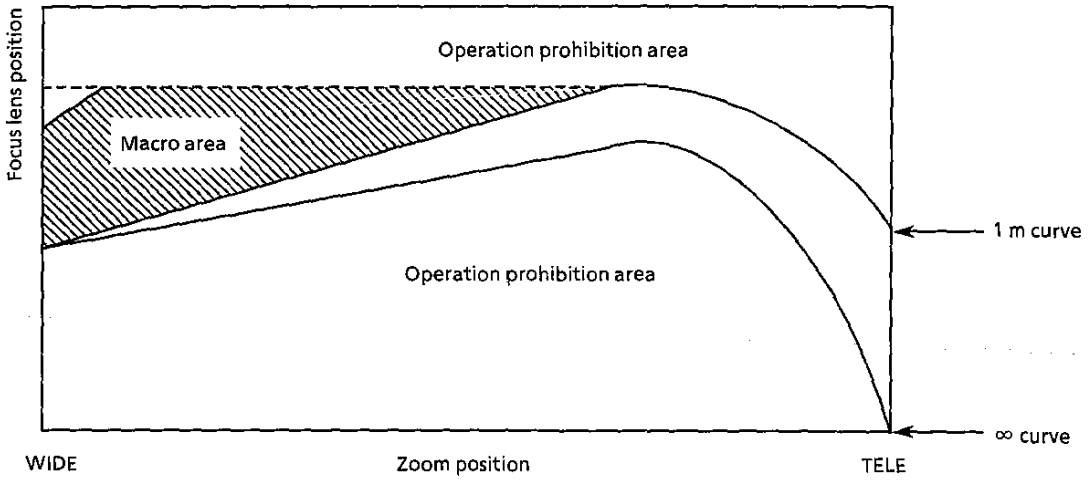


Figure 9-3. Relation between zoom lens and focus lens

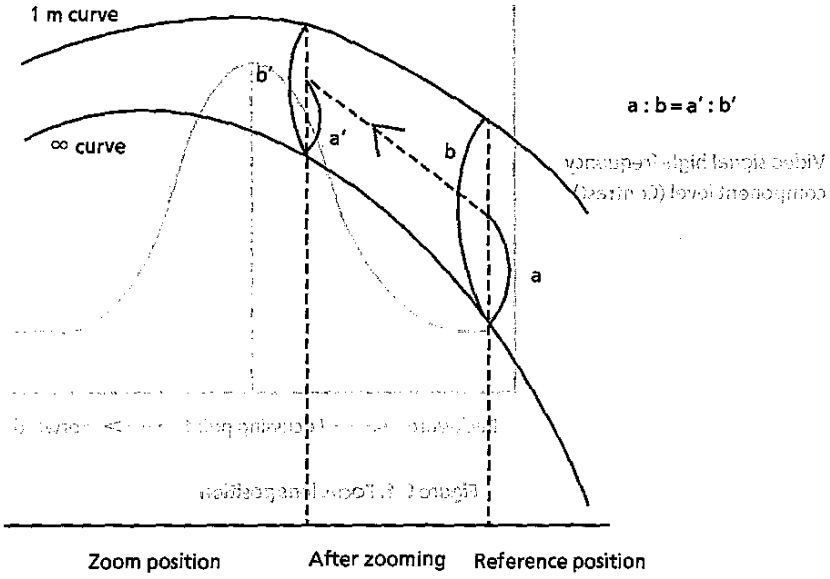


Figure 9-4. chematic diagram of tracking correction

9-2. Focus motor

The stepping motor drive speed is controlled by varying the cycle of driving pulses available at output pins (36) and (37) of the D/A converter that is incorporated in the camera microcomputer. The pulses' high and low levels are changed to control the slopes of the trapezoidal waveform. (Fig. 9-5)

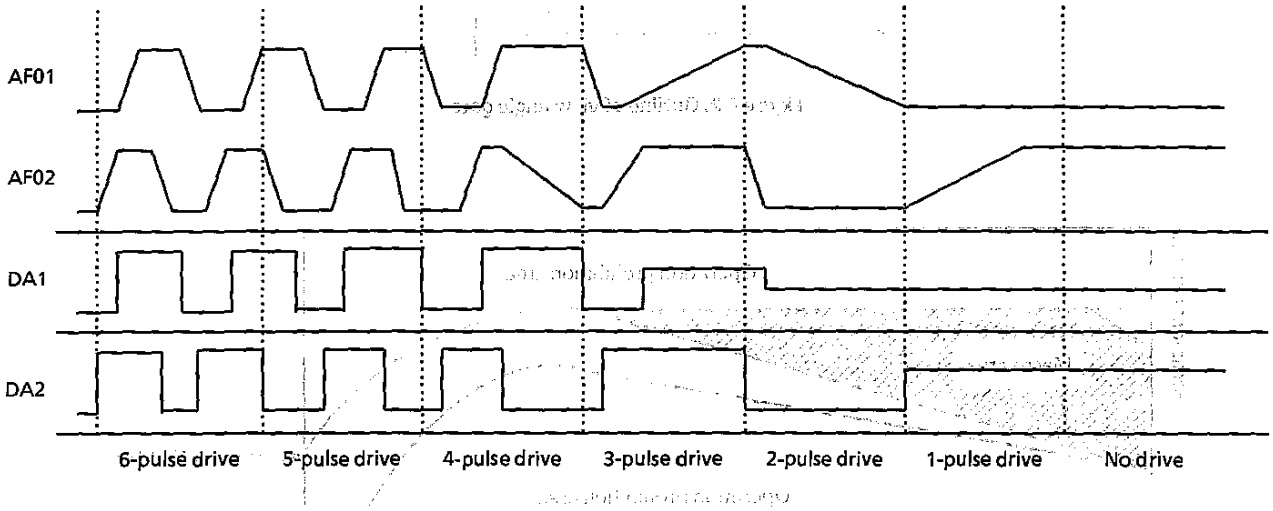


Figure 9-5. Driving pulses from microcomputer and motor driving pulses

The DA1 signal is converted into slope pulses by Q571, Q568, Q569 and C582. The DA2 signal is done so by Q565, Q564, Q566 and C581. The resulting signals are fed to pins (6) and (3) of IC552, respectively.

In IC552, the waveforms of the input signals at pins (6) and (3) are amplified to generate AF01, $\overline{AF01}$, AF02 and $\overline{AF02}$ pulses, which are used to drive the stepping motor. Q567 and Q570 form a protective circuit for IC552.

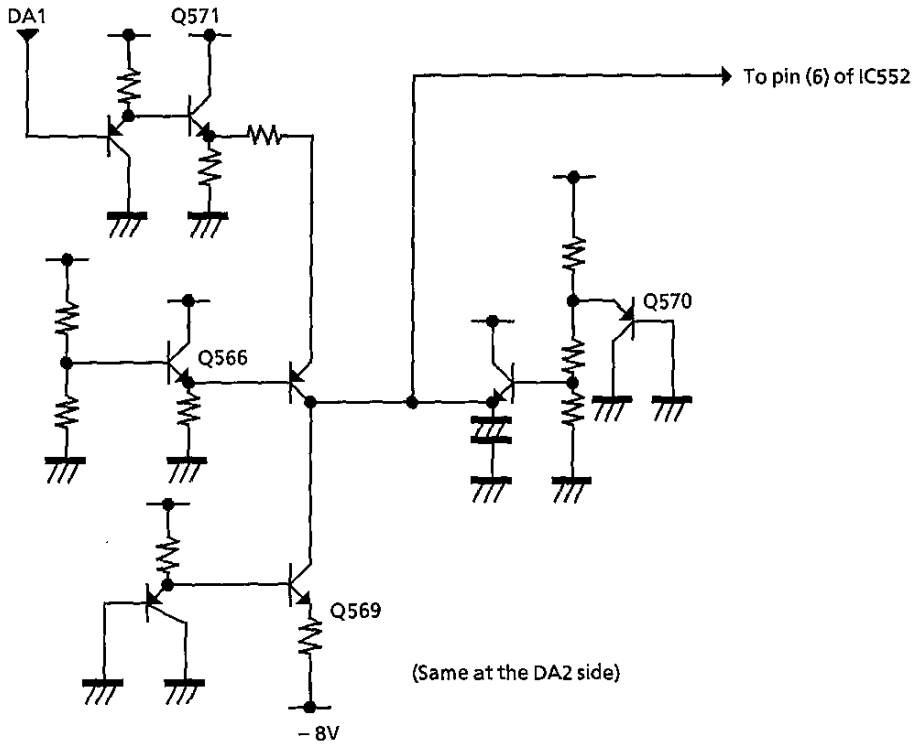


Figure 9-6. Focus drive slope control

9-3. Zoom motor

The driving pulses at output pins (44) and (45) of the D/A converter that is incorporated in the camera microcomputer are fed to pins (2) and (7) of the zoom stepping motor driver IC (IC554). The power control signal (ZC) too is sent to this IC at the same time.

The driving cycle is 180 pps in the normal operation. At the TELE end position, however, the cycle gets shorter from 120 pps to 60 pps. (Fig. 9-7)

To cope with operating noises, when the signal at pin (43) (Z speed) becomes high, the camera microcomputer activates capacitors C578 and C579, connected with pins (3) and (6) of IC554, to ease the slopes. (Fig. 9-8)

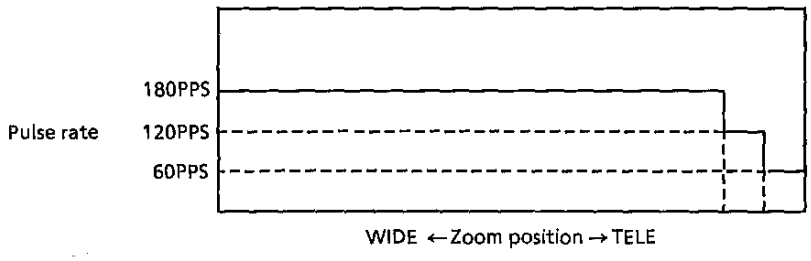


Figure 9-7. Zoom speed change

"H" ---- Low speed (Line ----- shown below) Normal operation
"L" ---- High speed (Line —— shown below) At power-on or adjustment

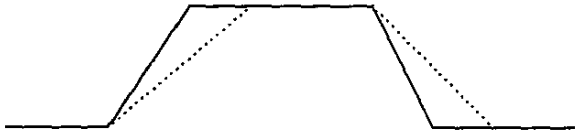


Figure 9-8. Zoom driving signal waveform

9-4. Photo interrupter

The photo interrupter is used for setting the reference focus lens (rear lens) position and zoom position.
The photo interrupter detects the edge of the screening plate which moves along with the focus lens to amplify its voltage variation in IC551. The amplified signal is inputted to A/D by the camera microcomputer.

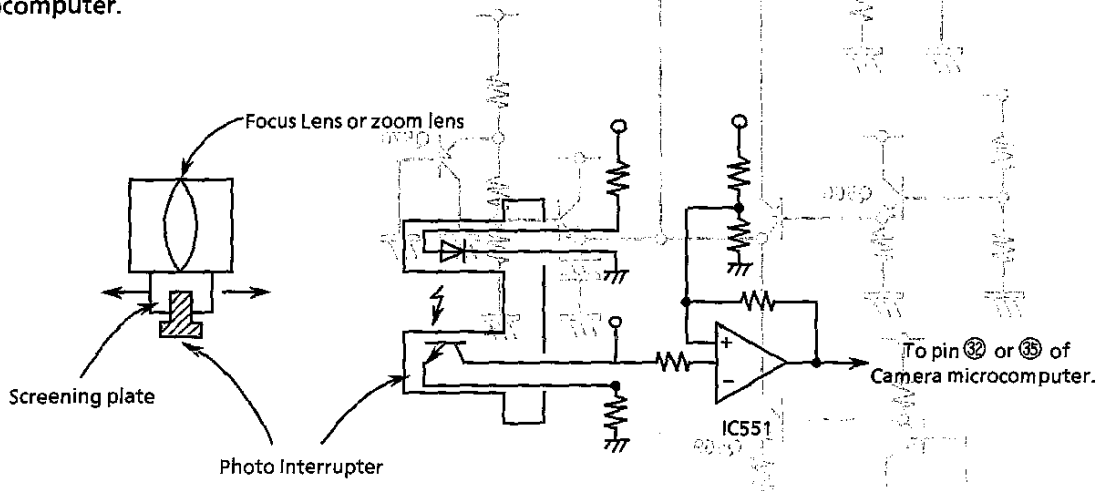


Figure 9-9. Photo interrupter block diagram

9-5. Hall sensor

The hall sensor built in the iris meter outputs a magnetic field variation caused by the variation of the working angle of the iris meter, in the form of a voltage.
The voltage variation is amplified by IC1504 before sending it to the camera microcomputer as a voltage signal that indicates the state of the iris.

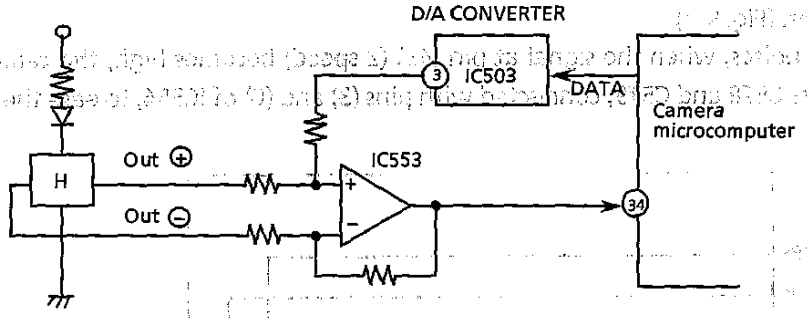
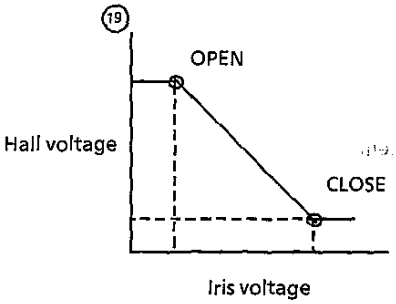


Figure 9-10. Hall sensor block diagram



Since the output from the hall sensor varies widely, with the basic adjustment of the iris, the hall voltage and the iris voltage when the iris is fully open and when it fully closed are sent respectively to the camera microcomputer to be stored in memory.

(2) IC272 (blurring microprocessor) description

IC272 receive the movement vector data and accumulation data from IC271 (hand blurring detection IC) and sends the data necessary for processing of IC271.

The processing steps of the blurring microprocessor are shown in the flowchart in Fig. 11-3.

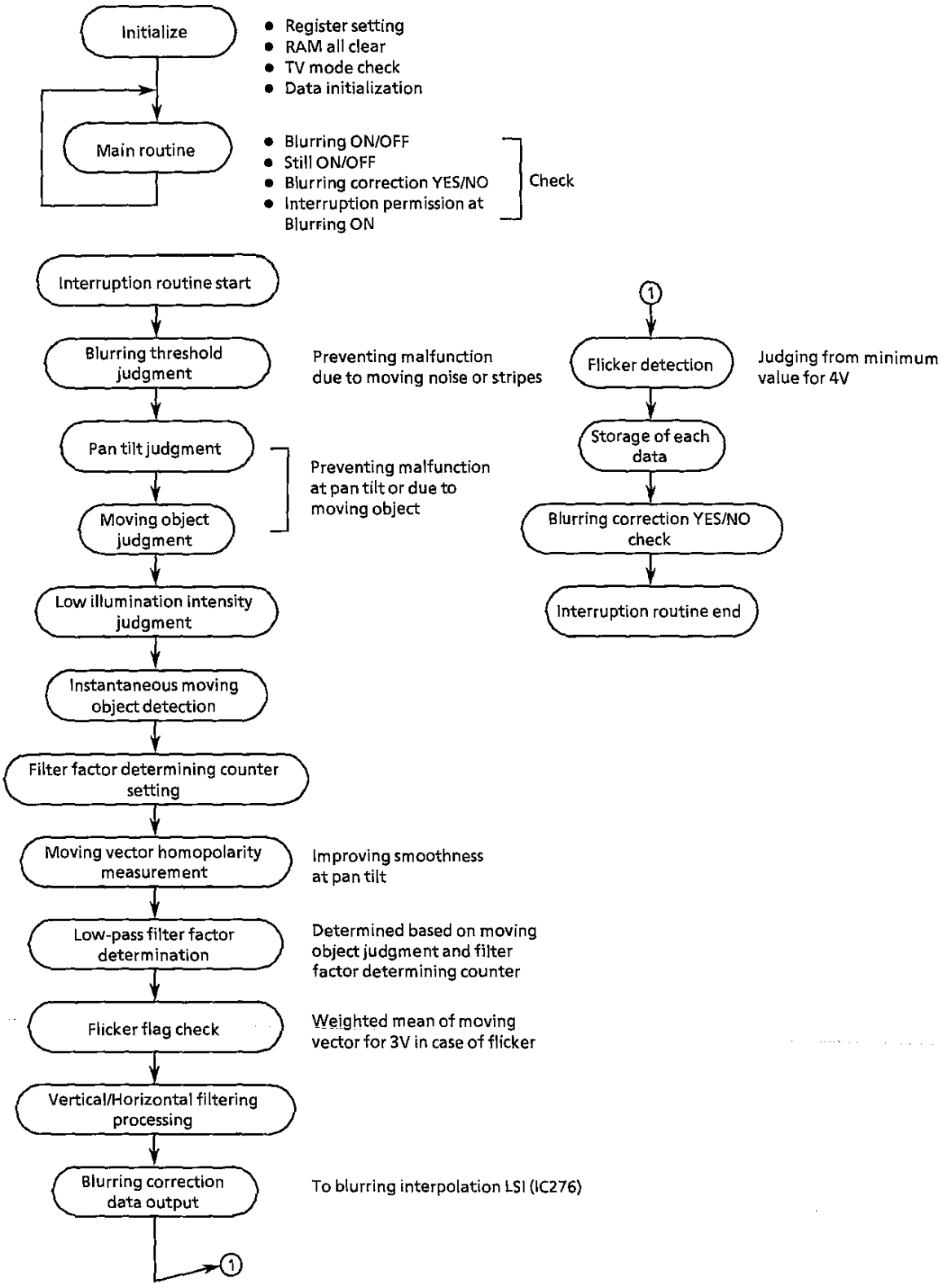


Figure 11-3. Blurring microprocessor processing

(3) IC276 (blurring interpolation) description

IC276 is composed of a memory control section and interpolation section. The memory control section controls the field memory by means of the data from the blurring microprocessor. The interpolation section performs interpolation when magnifying the image.

First it writes the Y signal (8 bit) and C signal (4bit) from DPS in the field memory.

Then it receives the blurring data from the blurring microprocessor based on the information obtained from the blurring detection IC, and read out the image while correcting it according to the blurring amount.

As the data read out from the field memory is 6/7 times of the whole, one piece of image is made by means of interpolation.

Therefore, the image in blurring correcting operation is 7/6 times of that in normal operation.

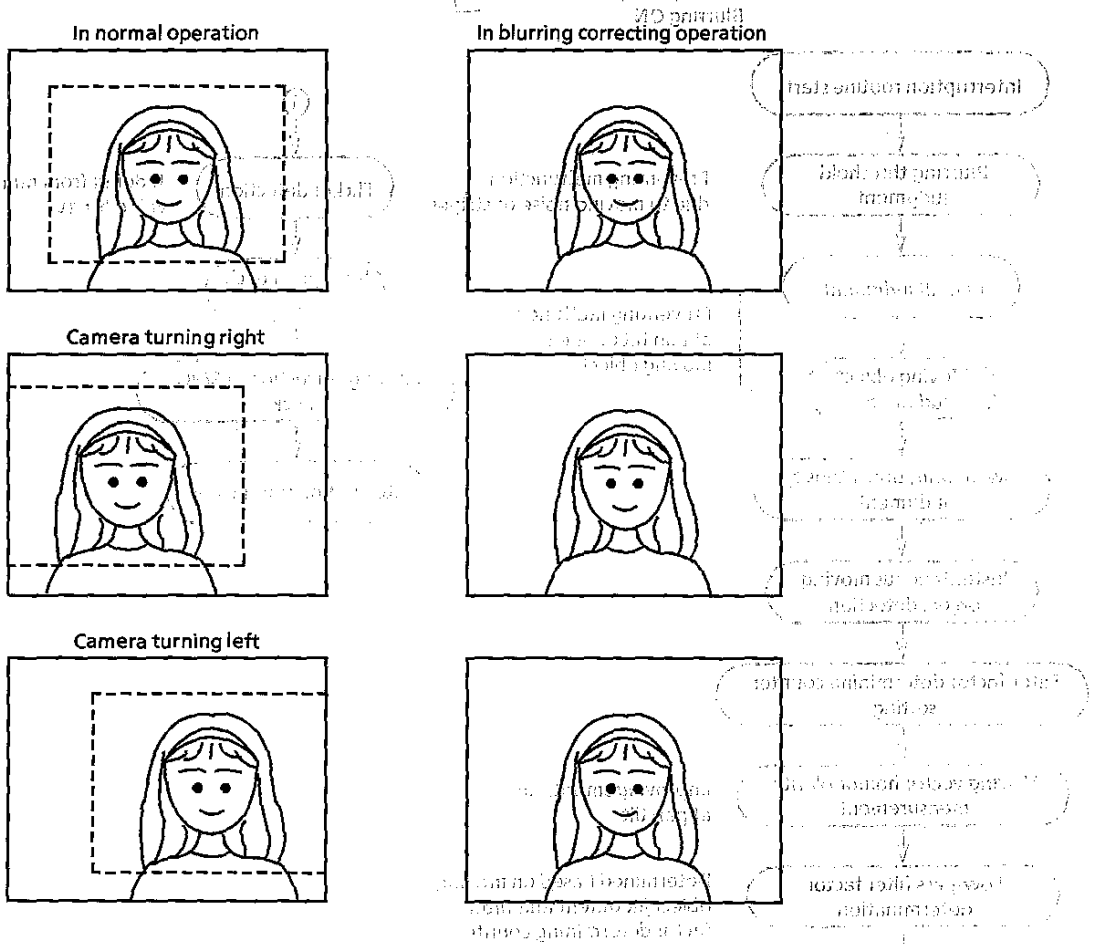


Figure 11-4.

As shown in the above figure, even if the camera moves right and left, blurring correction is made so that the object is picked up without blurring.

As to readout from the field memory, it is absolutely necessary to read out the data of the previous field. If it is not performed, in readout of a certain field, the previous field and the present field are read out at the same time, causing dislocation on the screen.

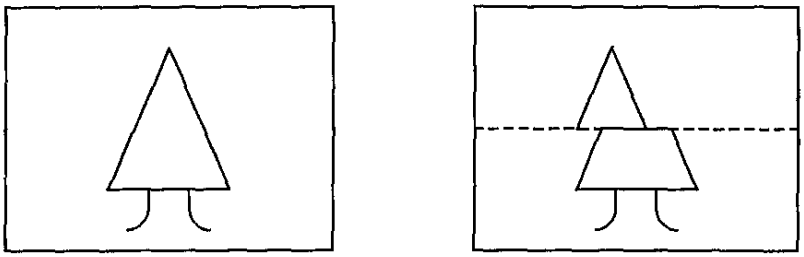


Figure 11-5.

Writing in the memory is started next to the readout endpoint.

For (n – 1) field, 0~242 (NTSC) 0~286 (PAL) are written in the memory.

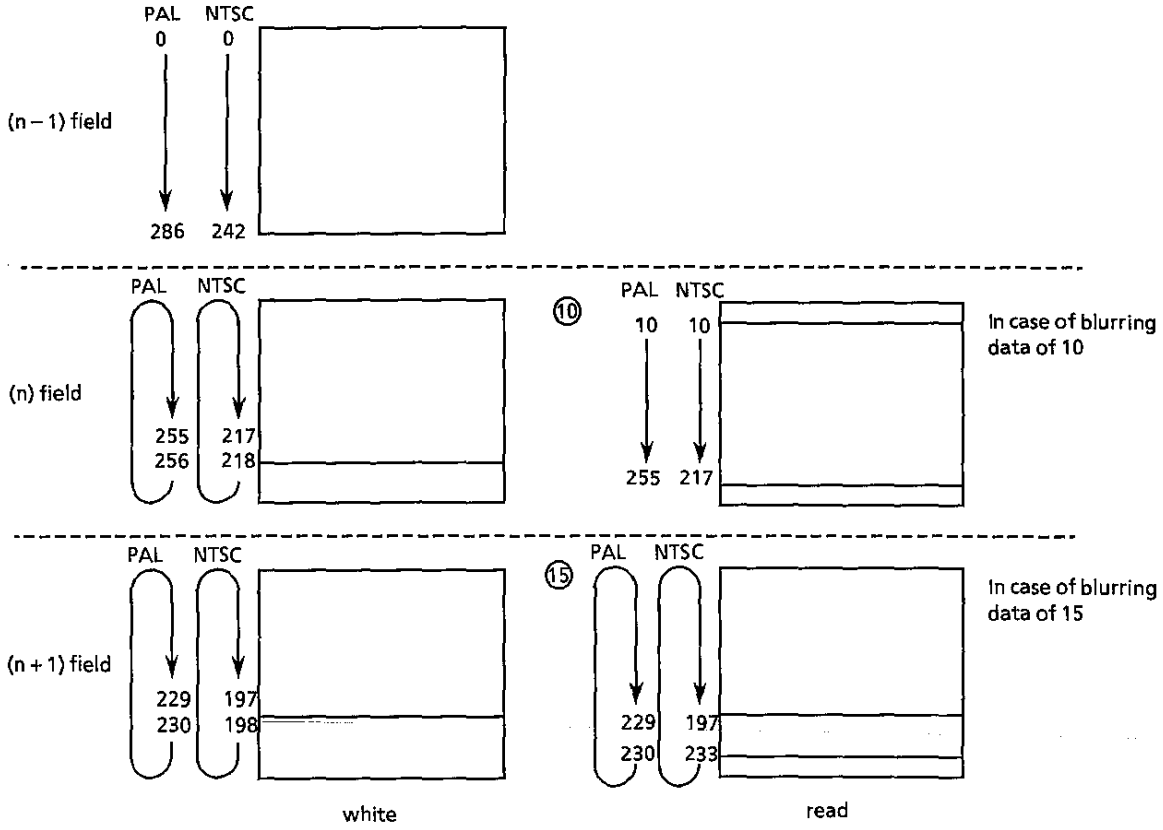
For (n) field, 10~217 (NTSC) 10~255 (PAL) are read out in case of blurring data of 10.

It is because:

$243 \times \frac{6}{7} = 208$ (NTSC), $287 \times \frac{6}{7} = 246$ (PAL)

$10 + 208 - 1 = 217$ (NTSC), $10 + 246 - 1 = 255$ (PAL)

Then, writing is started at 218 (NTSC) 256 (PAL) next to the readout end point 217 (NTSC) 255 (PAL) and 243 (NTSC) 287 (PAL) lines are written. As the memory is limited, resetting is made at 242 (NTSC) 286 (PAL), returning to 0 after 242 (NTSC) 286 (PAL).



A. How to use vertical memory

Figure 11-6.

For (n + 1) field, in case of blurring data of 15, readout is started at 233 (NTSC) 271 (PAL) because writing is started at 218 (NTSC) 256 (PAL) in (n) field.

218 + 15 = 233 (NTSC), 256 + 15 = 271 (PAL)

The readout end point is:

233 + 208 – 1 – 243 = 197 (NTSC), 271 + 246 – 1 – 287 = 229 (PAL)

Therefore, the writing start point in (n + 1) field is 198 (NTSC) 230 (PAL).

Passing is prevented by controlling the memory reading/writing as shown above.

As to interpolation, 7 is to be made from 6 data. It is realized by generating one new line by multiplying two lines by the factor as shown in the figure.

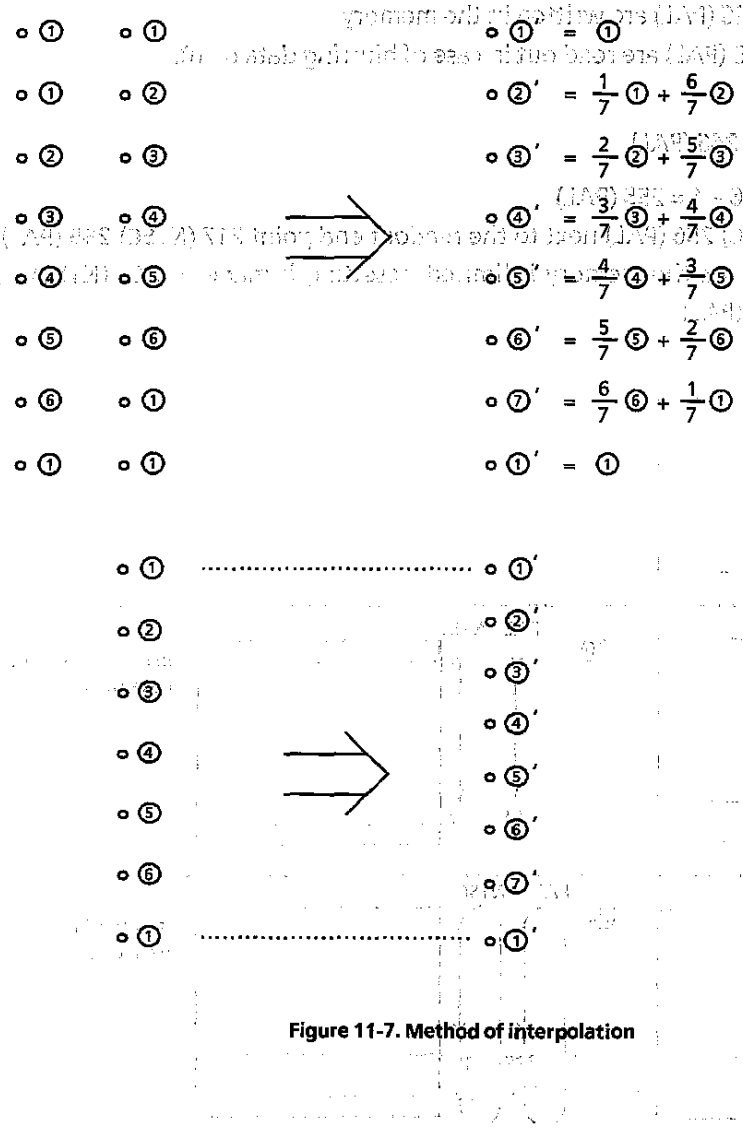


Figure 11-7. Method of interpolation

VCR SECTION

12. AUDIO CIRCUIT

12-1. Rough Description of Signal Flow

(1) Models VL-E30S/H, E40S/H

The input signal contains a mike signal which converts the sound mechano-electrically into a signal at the microphone. The mike signal, after its noise has been reduced, is FM-modulated and recorded at the rotary head together with chroma, tracking and luminance signals. (The mike signal consists of a signal from the built-in mike and one from the external mike.)

When the set is in the PB mode, the input signal, after the data from the rotary head has been converted magneto-electrically, becomes an FM signal. The FM signal, after its audio components have been taken out by the band-pass filter, is demodulated. Then, after the noise has been reduced, it is outputted to the AV pack or to the speaker or headphone by way of the amplifier.

(2) Other models (VL-E30X/E7E/E7D/E30U/C/E35U/E35)

The input signal consists of two systems; the mike signal which mechano-electrically converts the sound and the line signal which is inputted from the AV pack. The mike signal is selected when the camera is set to the CAM mode. The line signal is selected when the camera is set to the VCR mode. Input or output of the line signal can be switched on the menu screen. The mike signal or the signal from the AV pack, after the noise has been reduced, is FM-modulated and recorded at the rotary head together with chroma, tracking and luminance signals. (The mike signal consists of the signals from the built-in mike and the ones from the external mike.)

When the set is in the PB mode, the input signal, after the data from the rotary head has been magneto-electrically converted, becomes an FM signal. The FM signal, after its audio components have been taken out by the band-pass filter, is demodulated.

Then, after the noise has been reduced, it is outputted to the AV pack or to the speaker or earphone by way of the amplifier.

12-2. Flow of Microphone Audio Signal

The audio signal from the built-in mike unit is fed through pin (1) of connector P6601 on the mike amplifier PWB to pin (5) of the mike amplifier circuit IC6601. The audio signal from the built-in mike picks up mechanical noise. Therefore, it is amplified to eliminate the mechanical noise around 1.4 kHz (450 Hz for PAL) by means of the filter and fed into pin (3) of IC6501 on the main PWB.

Also, the audio signal from the external mike terminal is fed to pin (5) of the same IC. At this time, the potentials at pin (1) of socket SC602 (EXT MIC ON) are used to detect whether the external mike is in or out.

With the external mike plugged in, the external mike signal is automatically picked up; with the external mike unplugged, the built-in mike signal is automatically picked up.

The amplified audio signal from the built-in mike goes out of pin (1) and the signal from the external mike goes out of pin (7) and is fed to pin (38) of the audio signal processing IC602.

12-3. Flow of Line Input Audio Signal

* It should be noted that models VL-E30S/H are not provided with the external input function.
  When the "AV INPUT" mode is selected on the menu display, the signal coming via the AV pack is raised to its specified level of IC602 by means of R620 and R621. The resulting signal is fed into pin (36).

12-4. Flow of Recording Audio Signal

For the audio signal now in IC602, the mike audio signal from pin (38) is picked up in the CAM mode and the line input audio signal from pin (36) is selected in the VCR mode. It should be noted that models VL-E30S/H are not provided with the external input function. The ALC-controlled audio signal goes out of pin (33) through the low-pass filter in the audio band and is fed to pin (31). Then the signal goes through the noise reduction processing and is fed to pin (15). The resulting signal is fed to pin (16). Then, its level is limited to prevent over-modulation and FM-modulated at 1.5MHz to be outputted from pin (8) as an AFM signal. This REC AFM signal is mixed with chroma, tracking and luminance signals in the RF circuit. The final signal is then recorded on the tape.

12-5. Flow of Playback Audio Signal

The playback signal goes through the head amplifier and RF circuits into pin (1) of IC602. Only the audio components are picked up from the input signal by the 1.5-MHz band-pass filter. The resulting signal, after being amplified by AGC amplifier, passes through the switch. Then, with its AM components eliminated by the limiter, it is fed to the phase comparator to be demodulated. The demodulated signal, with its unnecessary components eliminated by the low-pass filter, goes into the sample hold processing (S/H). If the dropout time is too long, muting is held until the FM signal is detected. This signal undergoes the noise reduction process. Then it passes through the low-pass filter via pins (15) and (16), and is amplified after going out of pins (33) and (32) to be fed to pin (19).

12-6. Speaker/Headphone Circuit

The signal outputted from pin (19) of audio processing IC602, after its input level has been adjusted by R6403 and R6404, is fed to pin (2) of IC6401. IC6401 is the power amplifier IC with BTL (Balanced Transformer Less) system employed. It is provided with an electronic sound level control. After the sound level is adjusted by the level control signal fed to pin (4), the sound signal from pin (8) is outputted to the headphone (+) and the one from pin (5) is outputted to the speaker (−) via Q6401. Of the signals outputted from pin (5), the ones that go into pin (8) of SC602 are again outputted to the speaker from pin (9) of SC602 via the headphone jack. The speaker sound, with its signal turned on by Q6401, is let out only in the VCR mode. When the headphone is connected, the speaker sound is automatically cut off.

12-7. Audio Circuit Standard Level

Applied points	Applied points	Standard level [dBs]	Standard level [mVp-p]
Pin (5) of IC6501		−63	
Pin (3) of IC6501		−45	
Pin (7) of IC6501	C6504	−38	
Pin (1) of IC6501	C6505	−34	
Pin (38) of IC602	C609, R603	−38	
Pins (31), (32) and (33) of IC602	C640, TP605	−15	
Pin (19) of IC602		−8	
Pins (23) and (24) of IC602	C634	−15	
Pins (15) and (16) of IC602	C630	−15	
Pin (8) of IC602	C626, TP603		340
Pin (1) of IC602			600
Pin (36) of IC602		−21	
Pin (1) of IC603		−8	

13. DC-DC CONVERTER CIRCUIT/POWER CIRCUIT

13-1. OUTLINE

In order to make the unit smaller and lighter as well as to attain a higher efficiency, the switching frequency is set to approximately 480 kHz and the high capacitance ceramic capacitors are used for smoothing and other tasks.

Necessary voltages — CAM4.9V, CAM3.3V, CAM17.5V and – 13V for the camera section; LCD4.9V, LCD9V, LCD – 8V and LCD – 16V for the LCD section; and P-CON4.9V, PB4.9V and H/A4.9V for the system controller — are generated. As for the drum motor and capstan motor, voltages corresponding to their possible servo error signals are generated. In addition, BL5V is provided as a power source for the back light.

The unregulated voltage power source is directly used by the back light (BL5V), loading motor, system control circuit, camera zoom motor, etc.

13-2. CIRCUIT DESCRIPTION

(1) Control IC900 (MB3785V)

Ⓐ Reference voltage circuit

The temperature-compensated reference voltage (≒ 2.50V) is generated from the voltage supplied from the Vcc1 terminal (pin (18)). It is not only used as the power for the IC's internal circuits, but is taken out via the V_{REF} terminal (pin (19)) and resistive-divided to be used as each output voltage and as the reference voltage for each DTC terminal.

Ⓑ Triangle wave generating circuit

The stable triangle waveform of 480 kHz is obtained by connecting the timing capacitor and resistor to the CT terminal (pin (17)) and RT terminal (pin (16)), respectively and connecting the ceramic oscillator to the OSC terminal (pins (14) and (15)). The waveform amplitude is inputted to each PWM comparator in IC with 1.3-1.9 V.

Ⓒ Error amplifier

This amplifier detects the output voltage of the switching regulator and takes out the PWM control signal. The 1ch and 2ch are used for P-CON4.9V and CAM3.3V output voltage control, respectively; the 3ch and 4ch for drum motor and capstan motor speed control, respectively.

Ⓓ PWM comparator

- 1ch (for P-CON4.9V), 2ch (for CAM3.3V)
  It is a voltage comparator with two inversion inputs and one non-inversion input. It controls the output pulse ON time according to the error amplifier output. When both the error amplifier output voltage and DTC terminal voltage are lower than the triangle wave level from the oscillator, the output transistor is turned on.
- 3ch (for drum motor driving), 4ch (for capstan motor driving)
  It is a voltage comparator with two inversion inputs and one non-inversion input. When both the error amplifier output voltage and DTC terminal voltage are higher than the triangle wave level from the oscillator, the output transistor is turned on.
- The 1ch and 2ch use the DTC terminal for soft start.

Ⓔ Output circuit

The output circuit configuration is of totem pole type. By supplying the ON current and OFF current of the externally-added switching transistor, the switching transistor speed is increased. The ON current is controlled by the resistor and capacitor externally added on the VE terminal (pins (47), (43), (41) and (38)); the OFF current by the capacitor externally added on the C1 terminal (pins (1), (3), (34) and (36)) and C2 terminal (pins (48), (2), (35) and (37)).

Ⓕ Timer latch type short protection circuit

The SCP comparator detects the output voltage level of each comparator for output short detection. When one comparator output level becomes 2.1 V or more, the timer circuit is actuated to start to charge the protection enabling capacitor externally-added on the SCP terminal (pin (23)). If the comparator output voltage does not return to a normal level before the capacitor voltage rises up to the transistor base-emitter junction voltage (≒0.65V), the latch circuit is actuated to turn off the output transistor and set a dead time of 100%. If the protection circuit is triggered, resetting can be made by turning on the power supply again.

Ⓖ Low-input-voltage malfunction prevention circuit

In the transient state after turning the power on, or at an instantaneous drop of power supply voltage, it detects the internal reference voltage level according to the power supply voltage and sets the latch circuit to turn off the output transistor, set a dead time of 100% and keep the SCP terminal (pin (23)) at "L" level. Resetting is made when the power supply voltage exceeds the threshold voltage of the low-input-voltage malfunction prevention circuit.

(2) 4.9V regulator circuit

The OUT(A) signal (pin (46)) of IC900 is added to the base of Q903 (2SB1386-R) and the pulse current is supplied to L901 (22 µH). During the off period, it passes through the feedback diode D900 (SFPB54) and is smoothed by C929 (3.3 µF). The resulting signal is then fed to the LC filters (L902-L905, L910, C932-C935) and is divided into P-CON4.9V, PB4.9V, LCD4.9V, CAM4.9V and H/A4.9V. Feedback to IC900 is made with P-CON4.9V and the dividing is made by R934 and R935.

PB4.9V is switched in Q9903 (2SB12956) and becomes on when the "PB-L" signal is sent from the system controller. CAM4.9V is switched in Q907 (2SB1320S) and inverts the "CAM CTL" signal in the inverter Q906 (DIC144EE) to make it on. Also, from P-CON4.9V, the power is outputted from Q9901 as an optional power source.

(3) CAM3.3V regulator circuit

The circuit behavior is the same as the 4.9V regulator circuit. Using transistor Q915 (FP101) (with a built-in diode), smoothing is made in L912 (22 µH) and C951 (2.2 µF). Though other systems start operating by adding P-CON6V to CTL1 (pin (20)) and CTL3 (pin (22)) of IC900, this circuit rises by means of CAM CTL (approximately 180 msec later than P-CON6V).

(4) CAM17.5V, LCD9V, LCD – 8V, – 13V and LCD – 6V regulator circuit

Though all the other circuits use the chopper method, this circuit adopts the flyback method (back boost) because it performs boosting and inversion. IC901 (MB3775FV) is a slaving IC. Supplied with the reference voltage and triangle wave from IC900, it rises using P-CON6V as the power supply. As the output type is "open collector", the transistor array and Q917 (XPI601) are used in "totem pole form" in order to increase the speed, waveform adjustment is performed, and "storage capacitor" is taken out and added to the base of Q908 (2SB1121T). The collector current of Q908 is once stored in T900, and supplied to each smoothing circuit via D901 (IMNi10) as a flyback pulse when Q908 is off. Feedback to IC901 is made by performing resistive dividing of the -8V circuit with R942, R943 and R947. In addition, control R943 is used for fine adjustment of the voltage so that +17.5V can be obtained. As CAM17.5V is to rise later than CAM3.3V, Q9906 (UMB2) is turned on by approximately 16 msec.later by the base resistor and capacitor of Q9907 (2SC4738Y). – 13V is used for turning on Q9908 (DTC144EE) by another 4 msec. later than C9904 and R9911. LCD9V is generated by dropping 17.5V by means of R9905 (zener diode D9901).

② Shutter pulse timing

Figure 5-4 shows the timing chart between OFD (pin ⑩ of the CCD image sensor) and øV1 pulse (pin ⑫ of the CCD image sensor) in each shutter speed. Figure 5-4 indicates that, after the sensor read-out, the exposure time (charge accumulation time) for the following read-out can be varied by the number of ΔVsub pulses following the sensor read-out pulse.

In this model, pin ㉑(OFDX) of IC1 (CCD timing generator) sends out ΔVsub pulses corresponding to the preset shutter speed, which is supplied to pin ② of IC2 (V-driver). After being amplified in IC2, the pulse is sent out from pin ⑲(Vsub) of IC2. It is then overlaid on the OFD voltage and supplied to pin ⑩ of the CCD image sensor (IC1001).

Refer to Chapter 4 (Description of Circuits) for details of shutter speed setting.

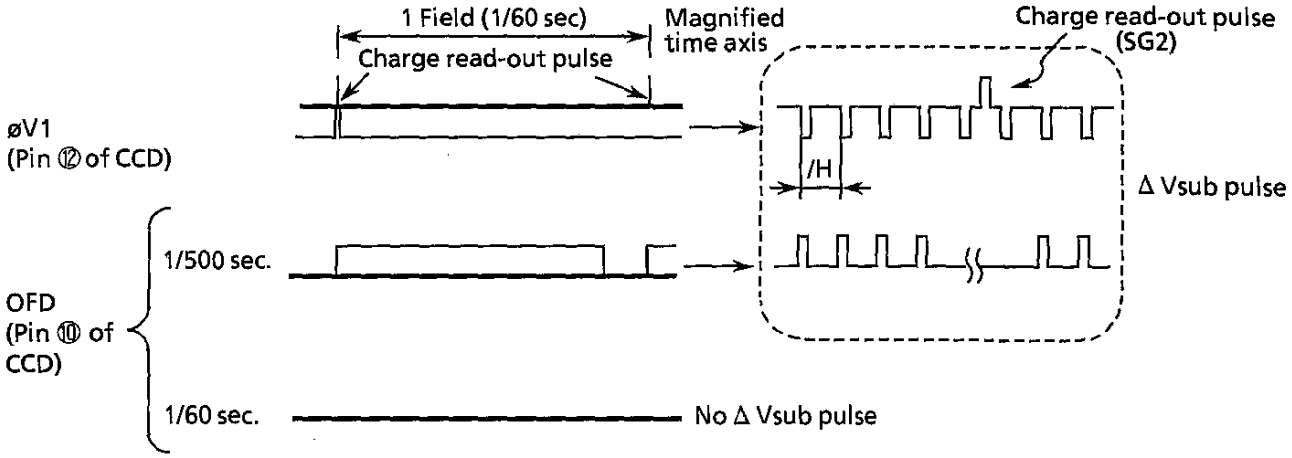


Figure 5-4. Timing Chart for Each Shutter Speed

5-4. Drive pulse timing

① Vertical drive (4-phase drive)

Due to the arrangement of the color mosaic filter, the read-out is made by changing the pulse timing of øV1, øV2, øV3 and øV4 at the start of the old and even field. During the normal transfer, the drive frequency is 15.734 KHz.

Figure 5-5 and Figure 5-6 show the timing charts for vertical transfer and charge read-out respectively.

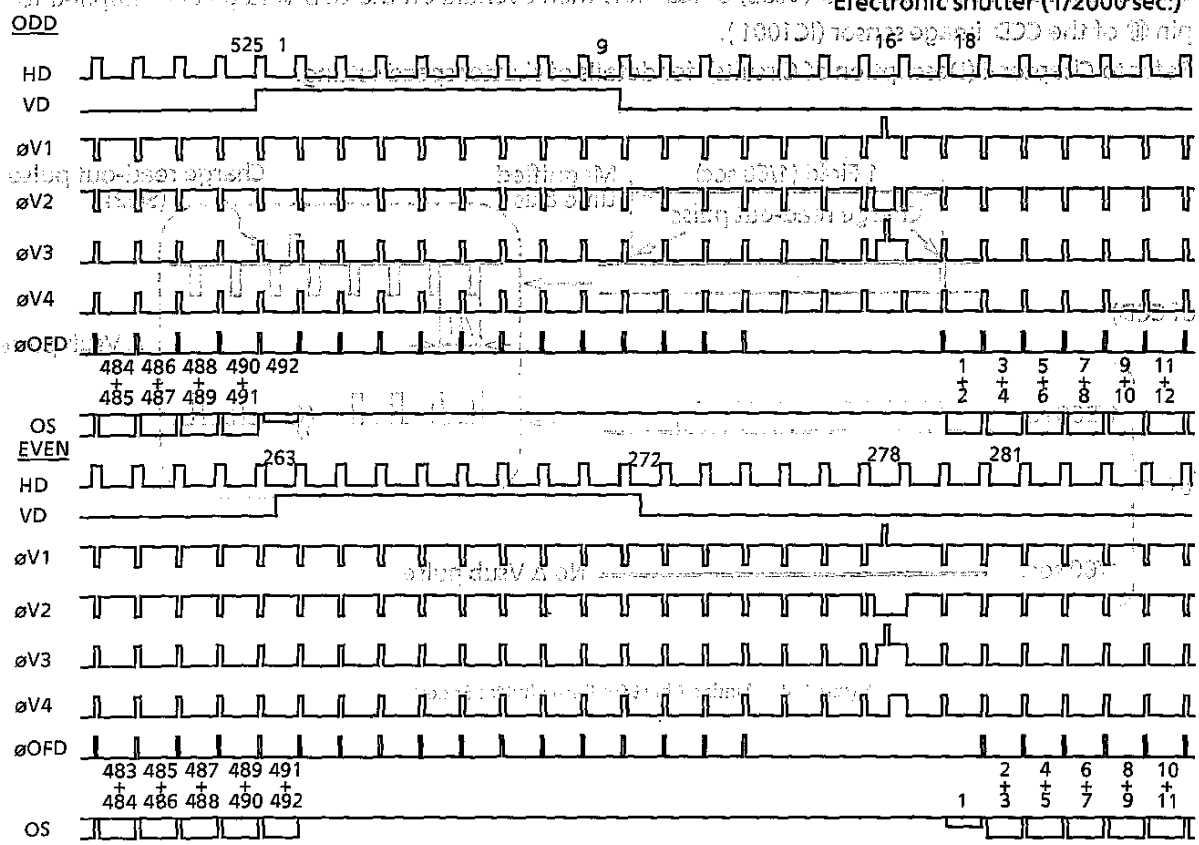


Figure 5-5. Vertical Transfer Timing Chart

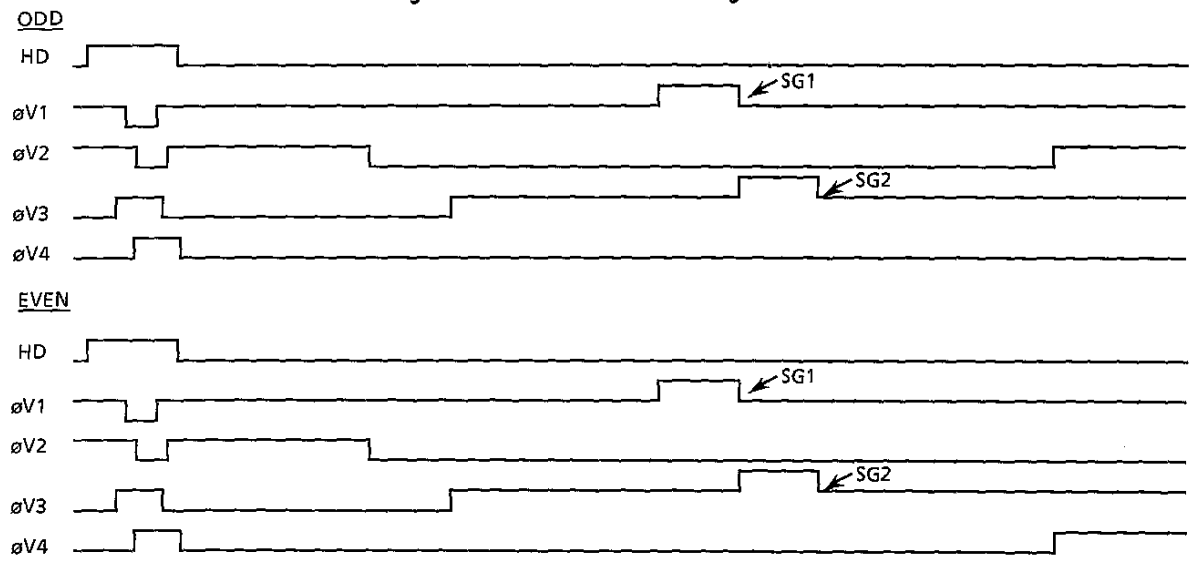
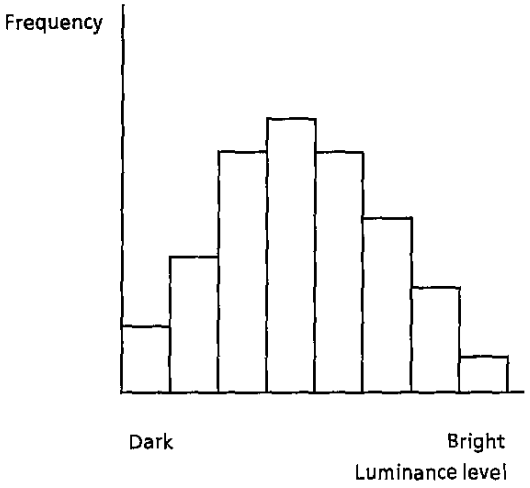


Figure 5-6. Charge Read-Out Timing Chart

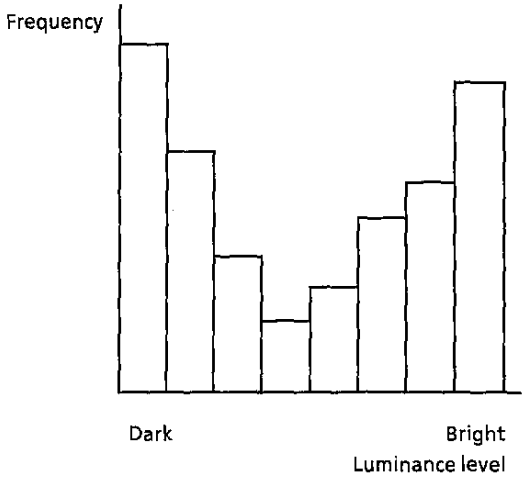
10. AE

10-1. Outline

This neuro-AE system, when the display is divided by 8 × 8 into 64 pieces of data in the luminance histogram, shows the luminance frequency distribution where the normal light, and the inverse light and excessive normal light have the following characteristics as shown below.

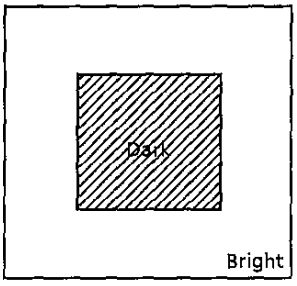


Luminance histogram for normal light

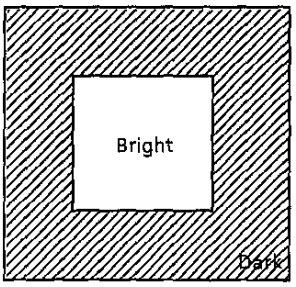


Luminance histogram for inverse light and excessive · normal light

In addition, for the inverse light and the excessive normal light, the bright and dark positions in luminance on the display change as shown in the figures below.



When in inverse light



When in excessive normal light

As shown above, the iris and AGC are control by judging the luminance on the display through the neural net.

The roles of the digital auto LSI of the neuro-AE system and the camera microcomputer are as follows:

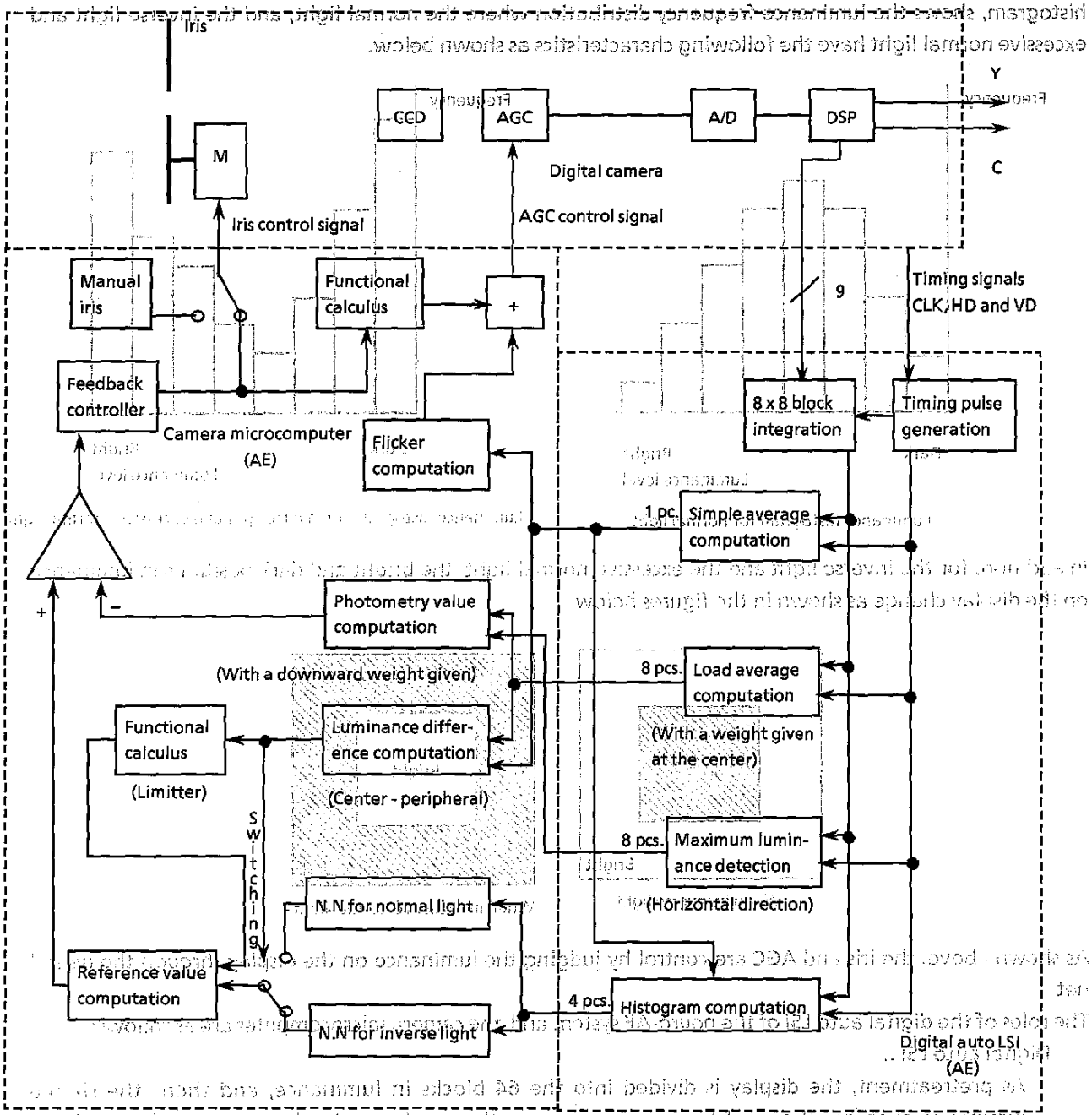
Digital auto LSI ...

As pretreatment, the display is divided into the 64 blocks in luminance, and then the simple luminance average, the load luminance average, the maximum luminance detection and the histogram processing are obtained from these divided 64 data.

Camera microcomputer ...

Each data from the digital auto LSI is used to correct the photometry values and the reference luminance for the correction of the iris. Also AGC is controlled by decreasing the flicker noises.

10-2. Neuro-AE system block diagram
(Camera microcomputer plus digital auto LSI)

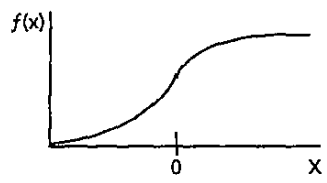


10-3. Construction of neural network and its learning

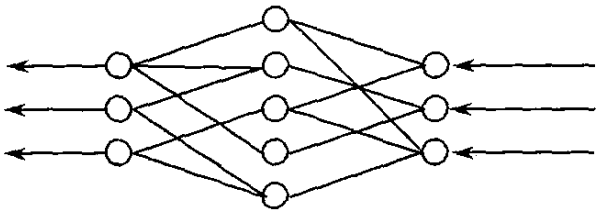
The neural network is made up of a combination of elements called neurons. As shown in the expression, a neuron adds the inputs together by attaching a weight to them and applies a non-linear function to the result thus obtained.

$$Z = f\left(\sum_{i=1}^{n} Wi \cdot Xi\right) \quad \text{..... Expression}$$

x: Input w: Combined weight
n: Number of inputs z: Output
f: Non-linear function as shown right



There are neural networks of various types. The one employed in this model is a type called the 3-layer perceptron. Figure 10-1 shows its construction. The above mentioned neurons are placed in the input layer, the middle layer and the output layer. The feature of the 3-layer perceptron is that any output/input characteristics can be obtained by adjusting the combined weight when the sufficient number of neurons are provided in the middle layer.



Output layer Middle layer Input layer

Figure 10-1. Construction of 3-layer perceptron

The process where the combined weight is adjusted to obtain a desired output/input characteristic is called learning. For the 3-layer perceptron, there is a learning method known as the back-propagation method, which is employed in this model. The following are procedures for this method:

(1) Prepare a desired set of an input and an output (as a tutor data).
(2) Place the input data prepared in Step (1) into the neural network.
(3) Calculate the output of the neural network.
(4) Compare the output of the neural network with the tutor data to obtain the difference between them.
(5) According to the difference, get the amount of adjustment of the individual combined weights by using another known expression.
(6) Change the individual combined weights by the amount obtained in Step (5).
(7) Repeat the procedures starting at Step (2) by using another tutor data.
(8) Repeat the procedures until the difference gets sufficiently small.

10-4. Configuration of neuro method

As the configuration of the neuro method, it has been devised that the neural network is inputted with the luminance histogram of the image, not with the image data. Since the data amount of the luminance histogram is small when compared with that of the image data, it is expected that the number of calculations of the neural network can be reduced. As shown in figure 10-2-(a), the luminance histogram is distributed around the average luminance for the image in the normal light, while as shown in figure 10-2-(b), the luminance distribution for the background and the object is separated in the inverse light and the excessive normal light. Accordingly, whether any correction is required can be decided by checking this pattern variations through the neural network.

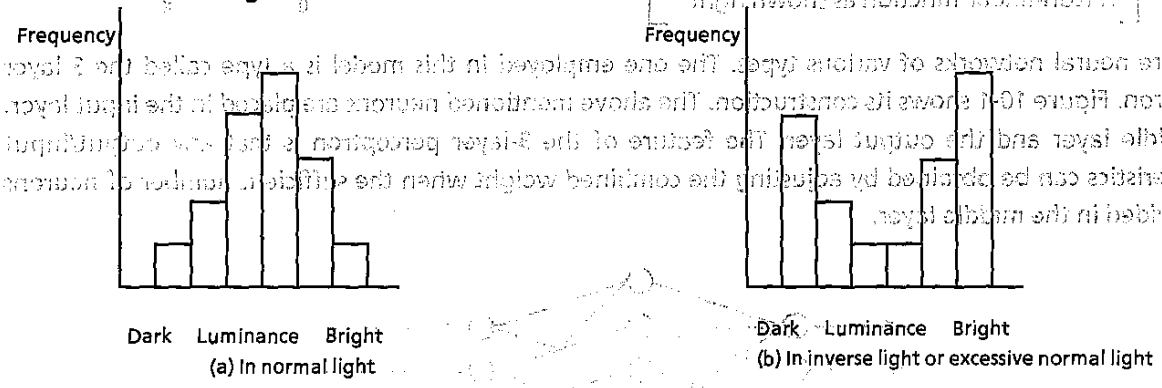


Figure 10-2. Typical pattern of luminance histogram

However, for the inverse light and the excessive normal light, both patterns have a similar distribution as shown in figure 10-2-(b), and it is difficult to discriminate one from the other by just looking at the luminance histogram. So, a proper discrimination method is required. For the neural network in this method, two networks are provided in advance for the inverse light and the excessive normal light so that the selection of the two network is made by the difference in luminance between the inside and the outside of the image. Figure 10-3 shows the block diagram.

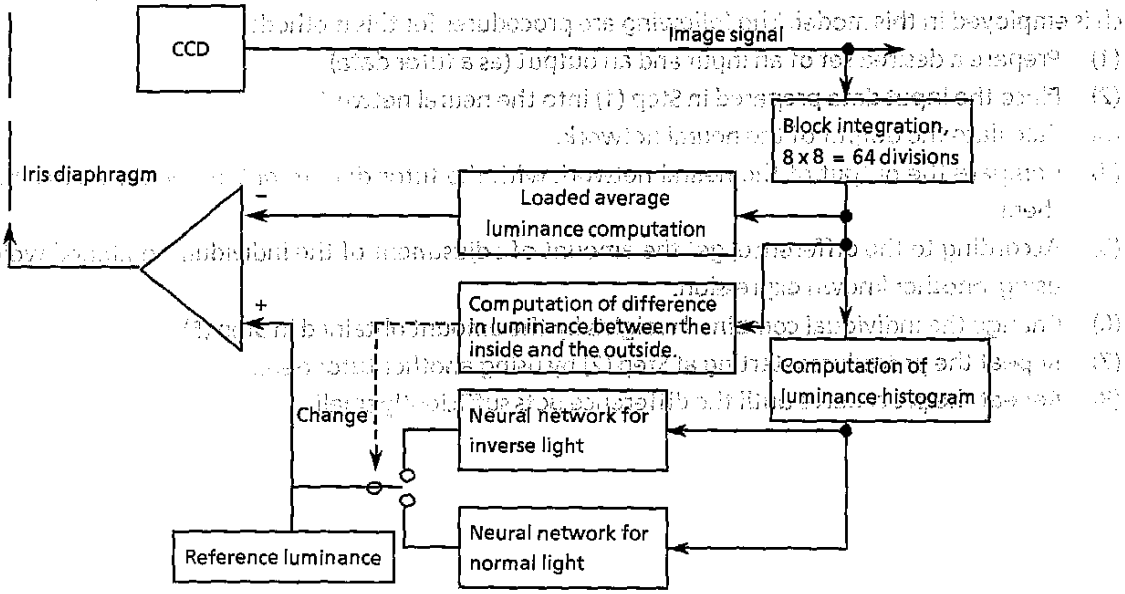


Figure 10-3. Block diagram

Explained next is the internal configuration of the neural network. Since an input reduces the number of calculations to the limit, as shown in figure 10-4, the area below the average luminance in the luminance histogram is divided into three sections with (average luminance/2) and (average luminance *3/4)in between them. And the number of blocks included in each section is made the inputs of the neural network. This is based on the fact that the luminance histgrams, in most cases, are symmetrical with the average luminance as an axis.

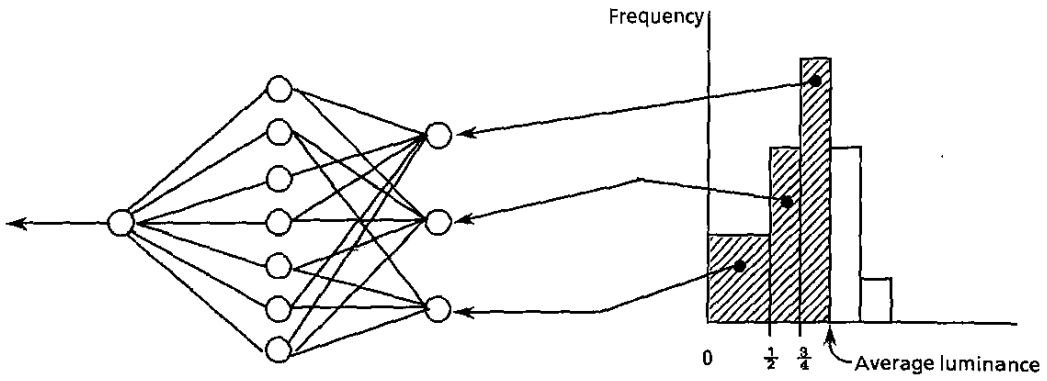


Figure 10-4. Inputs into neural network

For the number of neurons in the middle layer, since there is no difference found in the performance when checked while reducing the number of neurons from 100 down to 10, it is given 15 with the safety of the neural network operation in mind. The output layer which outputs the correction amount against the reference luminance is provided with one neuron. As a result, the configuration of the neural network is made up of three neurons for the input layer, 15 for the middle layer and one for the output layer.

10-5. Neuro-AE correction

The inverse light and the excessive normal light are discriminated by the AE method using the above mentioned neural network, and then fed back to the iris for control. However, there sometimes occurs an excessive neuro correction even though the object is not in so severe inverse light.

In order to prevent the occurrence of such a condition in this model, the limitter function is applied to the neuro output to control the excessive neuro correction.

10-6. Limitter function setting

① Insensitive area

In the area where there is a little difference in luminance between the center section and the periphery, that is, where the inverse light and the excessive normal light are not so strong, an insensitive area is provided to weaken the effect of the neuro correction.

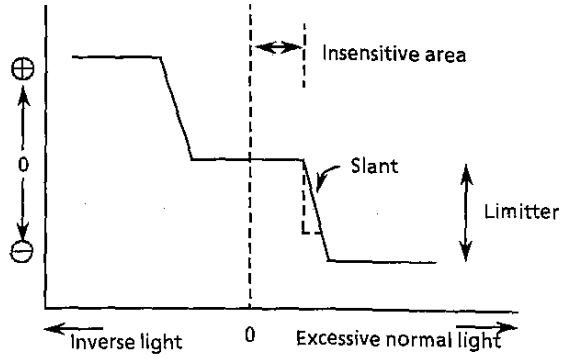


Figure 10-5. Limitter function

② Slant
A slant is given so that the gradual effect of the neuro correction is resulted in.

③ Limitter
Even in the area where the inverse light or the excessive normal light is strong, the limitter is provided to prevent the excessive neuro correction, instead of outputting signals with no processing.

By comparing the limitter correction value obtained from the graph above with the neuro correction value separately obtained by the neuro computation, either of the two whose absolute value is smaller is used as a final correction value to change the reference luminance.

10-7. Ratio of weights given at the AE center and in the lower section

In this AE system, the ratio of the weight given at the AE center and the coefficient of the downward weight are variable. The set values of this model are made based on the comparison with the existing models and the experience obtained in the entire AE system.

1. Weight given at the center
As shown in the figure 10-6-(a), the weight at the ratio of 8:5 is placed at the center with the coefficient of 1 at the center and 5/8 in the periphery given. A weight to be placed at the center is controlled by the digital auto LSI.

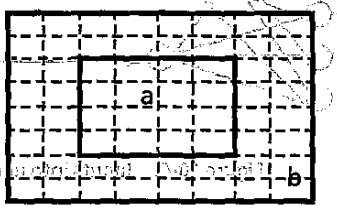


Figure 10-6-(a) a : b = 1 : 5/8

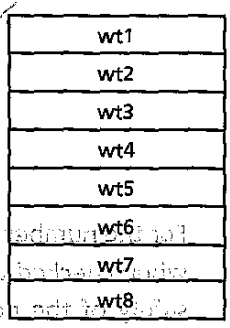


Figure 10-6-(b)

2. Downward weight
As shown in figure 10-6-(b), the display is horizontally divided into 8 equal sections and each section is placed with a weight.
In this setting, a weight is given as shown in figure 10-6-(c).
The control of the downward weight is made by the camera microcomputer.

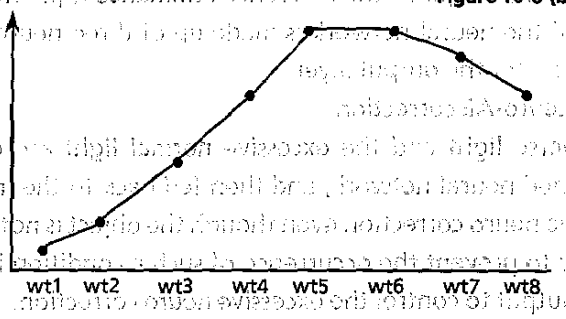


Figure 10-6-(c)

With the weights placed at the center and the lower each sections as shown in the steps 1 and 2 above, the setting is made so that the object that gets into the central area or the lower area can obtain a sensitive reaction.

11. DESCRIPTION OF HAND BLURRING CORRECTING OPERATION

11-1. HAND BLURRING CORRECTION

This unit has a hand blurring correcting function.

Correction is made while comparing with the data of the previous field using the Y signal.

Correcting operation is not made when the illumination intensity is low or a camera subject of low contrast is taken.

The blurring mark blinks when correcting operation is not performed.

Fig.11-1 shows the blurring correcting system block diagram.

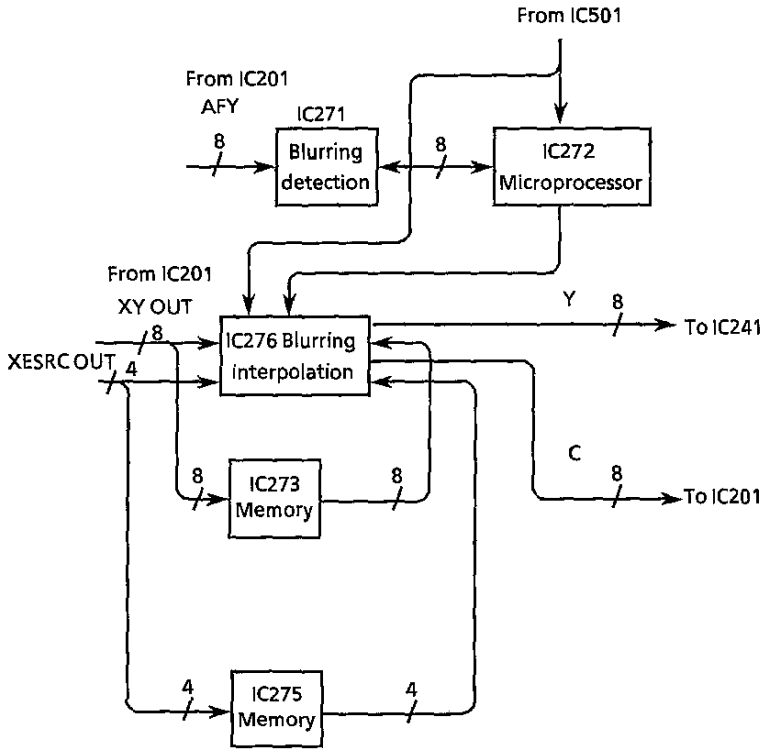


Figure 11-1. Blurring correcting system block diagram

(1) IC271 operation description

In IC271 the movement vector is detected using the AFY signal sent from IC201. The internal block diagram is shown in Fig.11-2 and the outlined description of each block is given below.

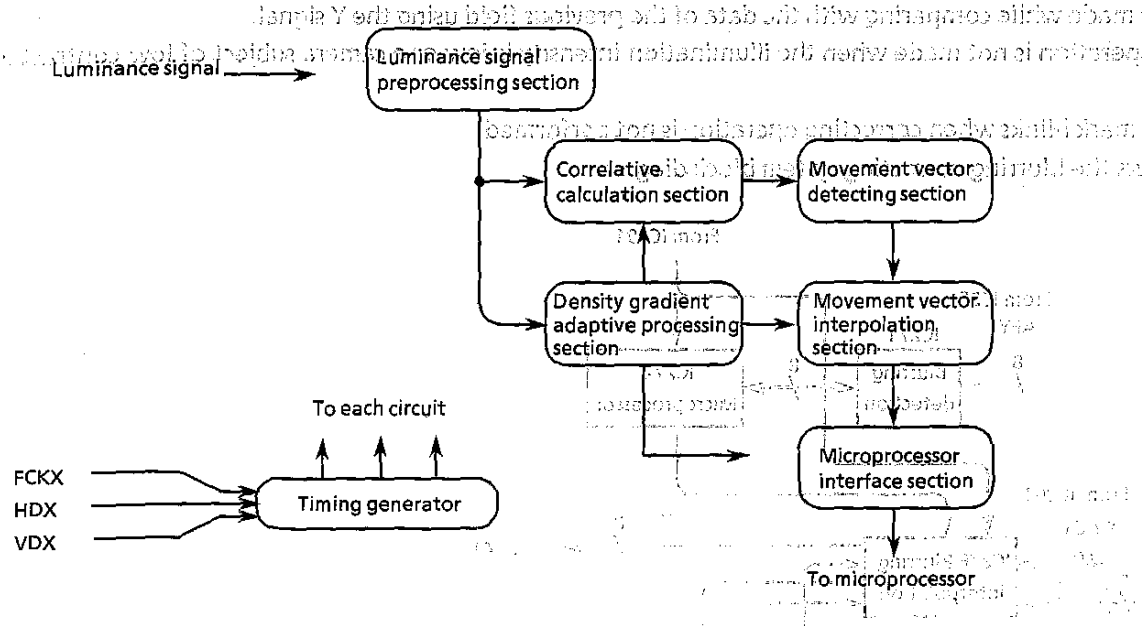


Figure 11-2. Blurring detection internal block diagram

- Timing generator
  The timing generator divides the image period of the inputted luminance signal into several blocks, assigns an address to each picture element for each block, and generates sampling timing such as representative point, density gradient component, etc.
- Luminance signal preprocessing section
  The luminance signal preprocessing section performs interpolation of the 1-line dislocation of odd field and even field in the vertical direction by the interlace method.
- Correlative calculation section
  It calculates the absolute value difference between the representative point of the previous field and the present field image, performs cumulative addition, and write it in the internal accumulation memory.
- Movement vector detecting section
  It detects the movement vector from the contents of the accumulation memory and sends it to the movement vector interpolation section.
- Movement vector interpolation section
  The movement vector interpolation section performs interpolation for improving the resolution of the movement vector detected in the detecting section.
- Density gradient adaptive processing section
  In order to obtain exact movement information from the video signal on which noise is superimposed, it eliminates flat blocks of low contrast from calculation so that calculation is made only using blocks having clear movement information such as edge portions.
- Microprocessor interface section
  Serial transfer is used for interfacing with the microprocessor.
  Therefore, in the interface section, parallel/serial conversion is performed, and reading and writing are made with the serial transfer clock from the microprocessor.

② Horizontal drive (2-phase drive)

Horizontal picture elements are transferred within a single horizontal scan time. The horizontal drive frequency is determined as follows.

$$\text{Horizontal drive frequency} = \frac{1}{\dfrac{\text{Effective horizontal scan time *}}{\text{Electrical effective number of horizontal picture elements}}} = \frac{1}{\dfrac{52.7 \times 10^{-6}\ (\text{sec.})}{503\ (\text{Picture elements})}} \fallingdotseq 9.54\ (\text{MHz})$$

* 63.56 – 10.9 = 52.7 (μsec.)

The frequency is approx. 9.54 MHz, enabling high speed operation.
øH1 and øH2 are square waves of 50% duty with 180° phase difference from each other.
Figure 5-7 shows the horizontal transfer timing chart.

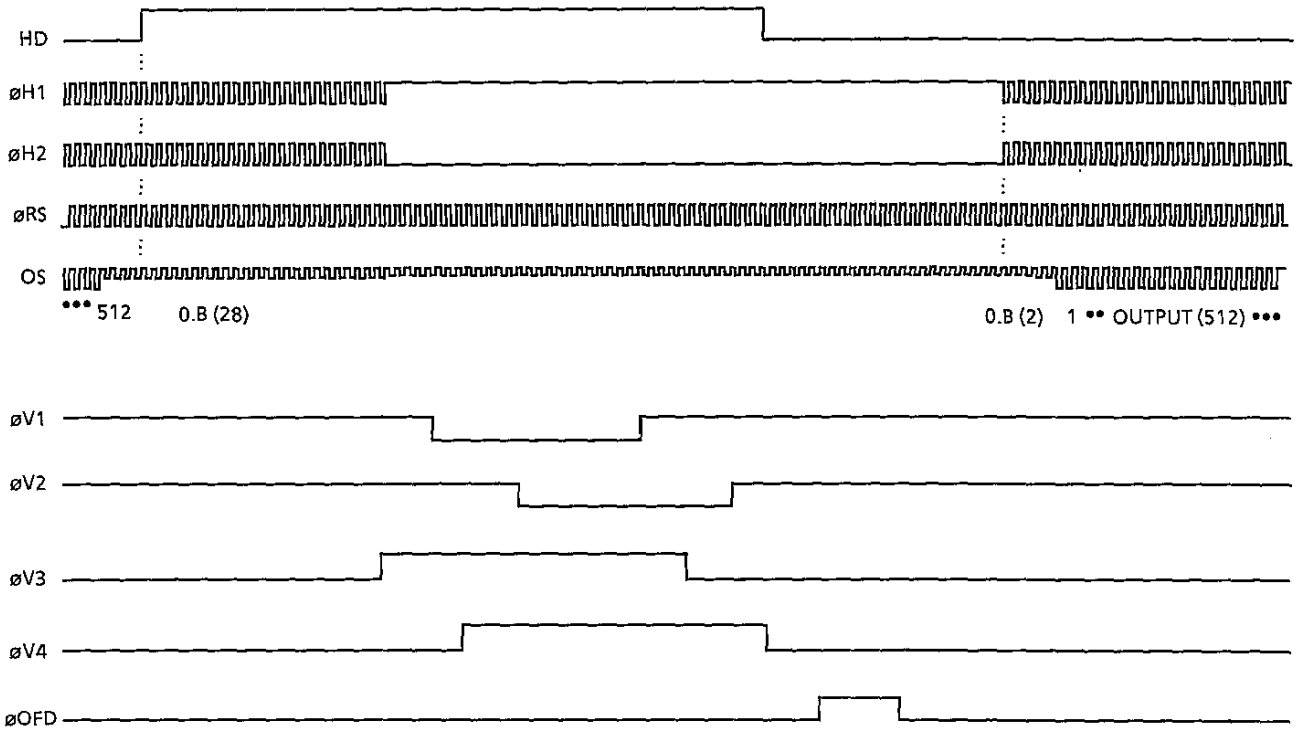


Figure 5-7. Horizontal Transfer Timing Chart

The signals C1 and C2 and the signals C3 and C4 are outputted in every 1H, and the interpolation signals are generated at CVL.P.F for synchronization.
For the subsequent operations to be processed in the unified system, R, G and B are placed in the 3-point sequential order.
For this, the point sequential signals of C1 C3, and (C2 + C4)and the 3-points sequential signals of C2, C4 and (C1 + C3) are generated to obtain the 3-point sequential signals of R, G and B by subtracting the both after multiplying Sr, Sg and Sb in the color separation block.
Create the following 2-point sequential signals of R-G and B-G from the 3-point sequential signals of R, G and B, and then create signals R-Y and B-Y from the following expression:

R-Y = Gry {(R-G) – Mry (B-G)}

B-Y = Gby {(B-G) – Mby (R-G)}

[Gry, Gby: Color difference gain]

[Mry, Mby: Hue]

(1) IC201 DSP (IX0171TA) Color block

- Data sent from A/D converter (IC102) is used as a signal delayed to 0H, 1H and 2H on 1H delay line.
  Signals C1 (= Mg + Ye) and C2 (= G + Cy), and
  signals C3 (= Mg + Cy) and C4 (= G + Ye)
  The above signals are outputted for each 1H, and synchronized by creating an interpolation signal on CVLPF circuit.
- CHLPF is applied with LPF to remove reflection by the subsequent subsampling circuit, while outputting signals C1, C2, C3 and C4 after synchronizing them.
- On subsampling circuit, the following two 3-point sequential signals are produced:
  C1, C3 and (C2 + C4), and
  C2, C4 and (C1 + C3)
- On color separation circuit, R, B and G are separated as the following expressions:
  $R = C1 - Sr \times C2$
  $B = C3 - Sb \times C4$
  $G = 1/2\{(C2 + C4) - Sg \times (C1 + C3)\}$

  However, at this time, color reproducibility can be corrected against the difference of CCD spectral specifications by changing the correction values Sr, Sg, and Sb of color reproducibility.
  R GAIN Adjustment address 50
  B GAIN Adjustment address 51

  When the above two GAIN are provided with G as reference at the time of white projection at 3200°K, white balance is adjusted so that G = R = B (vector center) is resulted by controlling R GAIN and B GAIN.

  Signals R, B and G as 3-point sequential signal carry out γ correction to be sent out to the subsequent step.
- On R-GøR-G GEN circuit, R-G and B-G 2-point sequential signals are created from R, B and G 3-point sequential signals.
- On color difference matrix circuit, when the following expressions are given:
  R-Y = Gry {(R-5) – Mry (B-G)}
  B-Y = Gby {(B-G) – Mby (R-G)}

  then, the color difference matrix R-Y and B-Y are made from 2-point sequential signals R-G and B-G.

Color difference gain correction value Gry	= R-Y Gain	Adjustment address 53
Color difference Gain correction value Gby	= B-Y Gain	Adjustment address 54
Color difference matrix correction value Mry	= R-Y MAT	Adjustment address 56
Color difference matrix correction value Mby	= B-Y MAT	Adjustment address 57

In the above four patterns, signals can be varied. Figure 7-8 shows the changes of the hue at this time.

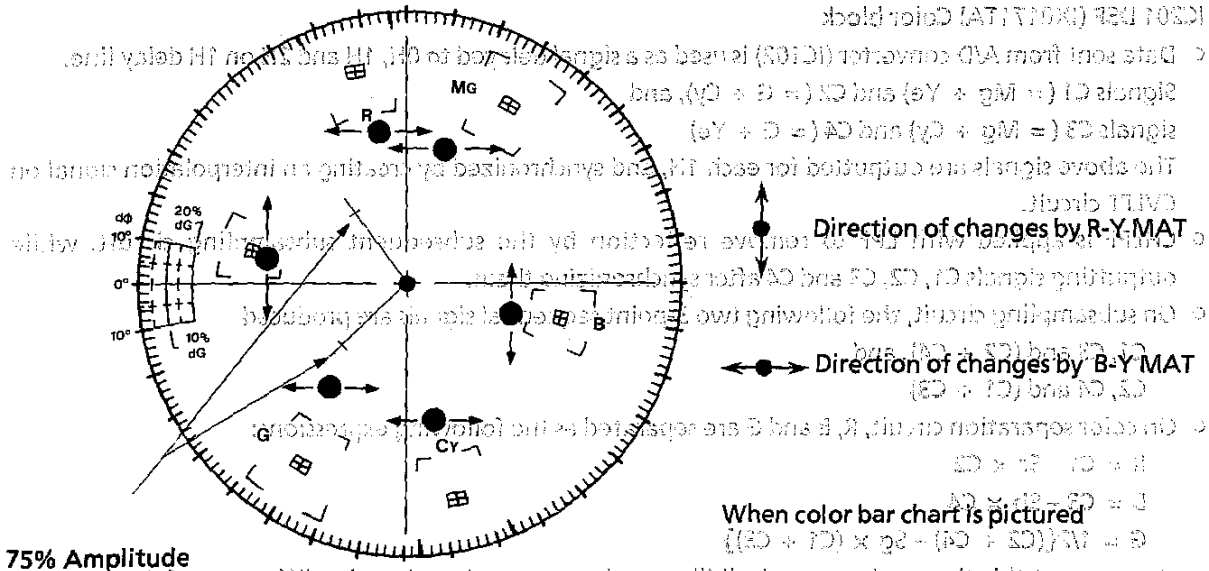


Figure 7-8. Hue Control

Each control of R GAIN, B GAIN, R-Y GAIN, B-Y GAIN, R-Y GAIN, R-Y MAT and B-Y MAT is made by sending address and data from the microcomputer through the interface with camera μ-CON (IC501) at pin ㉔ (DATA), pin ㉕ (DSPST) and pin ㉖ (CLK).

- The color difference matrix signals R-Y and B-Y carry out color modulation after mixing of burst with blanking section. Then, they are supplied to D/A converter (IC241) from pins ⑥⓪ to ⑦① as 8-bit digital macro signals (CDATA 0 to7).

(2) IC241 D/A converter (CXD1177Q) and peripheral circuits

Digital chroma signals (CDATA 0 to 7) outputted from DSP (IC201) are supplied to pins ⑨ to ⑯ of D/A converter IC, while clock signals (CDACLK) outputted from DSP are D/A converted by pin ⑳ before being sent out from pin ㉗ as analog chroma signals.

The chroma signals thus outputted go through Q243 low pass filter and Q244 peripheral band pass filter, and then they are sent out as camera chroma signals (CAM-C) to the EE circuit of VCR section through ⑲ pin FPC connected to SC19.

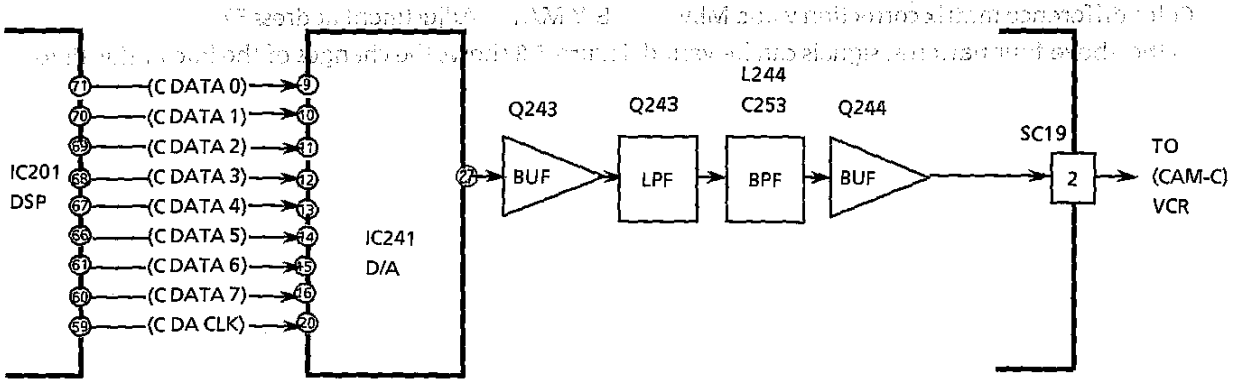


Figure 7-9. Chroma system IC241 peripheral circuit.

7. CIRCUIT DESCRIPTION (VL-E30U/C/E35U/E35, E40U/C)

7-1. Sensor circuit

Refer to Figure 4-5 for the sensor circuit block diagram circuits.

(1) Power source

Three power lines, +4.9V, +17.5V and −13V, are supplied from VCR to the sensor circuit.

① +4.9V line supplies power to the timing generator IC(IC1), 1820fH (=8FSC) oscillator (x1), and vertical driver (IC2).

② +17.5V power is supplied to VH of vertical driver (IC2). At the same time, after being stabilized to +15.1V at Q4, it is also supplied to CCD sensor and OFD voltage generator circuit (Q1, Q2, Q3 and Q4).

③ −13V line, after being stabilized to −8V at IC3, is supplied to pin ⑱ of vertical driver (IC2) as well as to pin ⑪ as P-well voltage of CCD sensor.

④ OFD voltage generator circuit, which utilizes 15.1V line power and vertical transfer pulse øV2 at pin ⑰ of vertical driver (IC2), generates 5.0V to 19V power by making adjustment at adjustment addresses 7B(H) and 7C(L) of D/A (IC1501).

(2) CCD drive timing generator IC (IC1)

Powered by +4.9V, this IC handles the digital signals of Low = OV and High = Vcc for both input and output. For reference clock signal, 910fH (4FSC = 14.31818MHz) is used. This clock signal is obtained by dividing by two the 1820fH (8FSC = 28.63636MHz) received from crystal oscillator (x1).

This clock signal is outputted from pin ㊶ as a CLK signal which is then sent to pin ㉙ of DSP IC (IC104) to be used to produce a sync signal for the entire camera section.

Pin ㉜ and pin ㉝ receive synchronized HD and VD pulses respectively from DSP IC.

① Horizontal transfer clock

FH1(pin ㉖) and FH2(pin ㉗) are pulses that perform one line of horizontal transfer during 1H scan. Their frequency is 9.54545 MHz and supplied to pins ⑧ and ⑦ of CCD (IC1001) as øH1 and øH2.

② Reset gate pulse

FR(pin ㉓) is a pulse to be used when changing the charge voltage of the sensor, and is supplied to pin ② of the CCD sensor with Low level clamped to 3.0V DC.

③ Vertical transfer clock and high speed shutter pulse

V1X(pin ⑱), V2X(pin ⑳), V3X(pin ⑰) and V4X(pin ⑮) send out pulses to perform one vertical transfer during 1H scan. Their frequency is 15.734 KHz. At the beginning of every field, the CCD sensor charge read-out pulses VH1X(pin ⑲) and VH3X(pin ⑯) are generated.

High speed shutter mode is controlled by the serial signals D0, D1 and D2 which are supplied from the camera microprocessor (Refer to Figure 7-1). During high speed shutter mode, pin ㉑ sends out OFDX corresponding to the shutter speed setting.

All of the above described signals V1X to V4X, VH1X, VH3X and OFDX, are sent out to the vertical driver IC(IC2).

Shutter speed (in sec.)	Serial data							
	D0	D1	D2	D3	D4	D5	D6	D7
1/500	1	1	0	1	0	1	0	0

External terminals are set as follows:

TVMD ② L ... NTSC mode
PSMD ⑥ L ... Serial mode
STEN ④ H ... Shutter mode
FLMD ⑤ H

External terminal serial data input timing

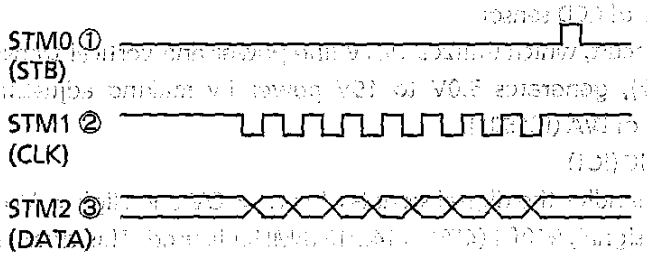


Figure 7-1. Electronic Shutter Control Chart

Synchronized with the rising edge of STM1 signal, STM2 data is shifted to take in 8-bit date. At rising edge of STM0 signal, the data is latched internally.
It is latched again at the falling of horizontal line HD1 signal when the charge read-out pulses (VH1X and VH3X) turn to be active.

(3) Vertical driver IC (IC2)

This IC generates the vertical register drive pulses øV1 to øV4 and the sensor charge draining pulse Vsub used for the high speed shutter based on the pulse timing supplied from the timing IC(IC1).

① øV1 to øV4 reverse and amplify V1X to V4X of the timing IC to make them pulses of Low = −8V and High = 0V. So far as øV1 and øV3 are concerned, VH1X and VH3X pulses (sensor charge read-out pulses) from the timing IC are overlaid on the vertical blanking period. These pulses have Low = 0V and High = 17.5V.

② Vsub regulator sends out a pulse (low = −8V, High = 17.5V) which is obtained after inverting and amplifying the OFD from the timing IC. It is then coupled with OFD power source at C1 and supplied to CCD image sensor.

(4) CCD image sensor (IC1001)

The CCD image sensor is composed of three major sections; a vertical shift register and sensor section, a horizontal shift register section and an output section. For details, refer to the descriptions on "5. CCD OPERATION."

The vertical shift register receives the transfer clock signals øV1 to øV4 (pins ⑫, ⑬, ⑭ and ⑮), while the horizontal shift register receives the transfer clock signals øH1 and øH2 (pins ⑧ and ⑦).

The output section receives +15.1V for the output transistor drain power source (OD, pin ①), and pulses of Low = 2V and High = 6.5V for the reset gate clock (øRS, pin ②).

The output signal is sent from the signal output terminal (OS, pin ④). it is then buffered at Q1001 and supplied to the subsequent IC101 (CDS, AGC:HA8144AF).

7-2. Luminance signal circuits

(1) IC101 (CDS, AGC) and peripheral circuits

CCD OUT signal sent out from the CCD sensor circuit is supplied to pin ㉟ of IC101.

The internal block of IC101 is made up as shown in Figure 7-2.

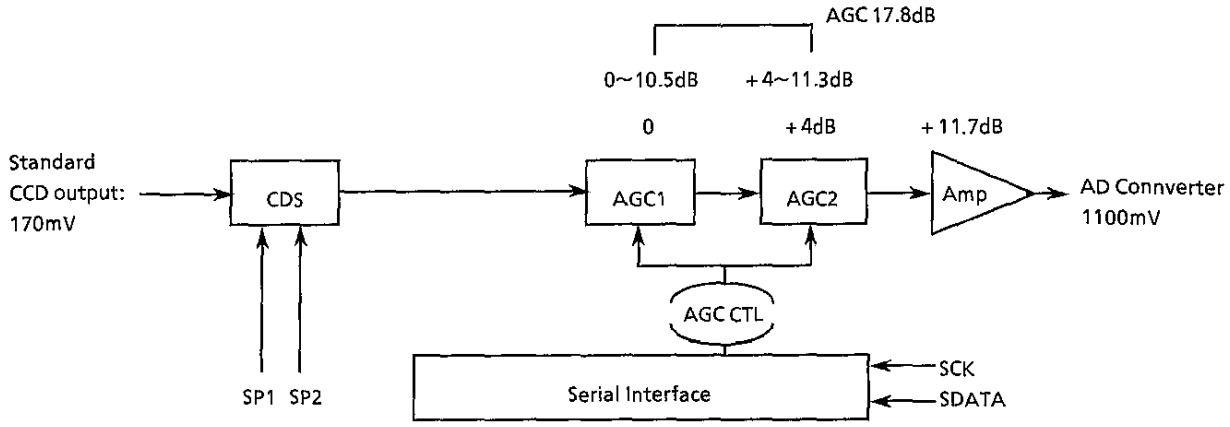


Figure 7-2

1) CDS (correlated double sampling) circuit

CCD image sensor sends out alternatively the noise section (signal for "A" period) and the signal section including noises in it (signal for "B" period). Major noises occurring in the image sensor are low frequency noises and overlaid on signals for output. Accordingly, this may result in the deteriorated S/N.

CDS circuit is made up of a clamp circuit, a sample hold circuit and an inverted amplifier, where low frequency noises are removed by clamping the noise section ("A" period) of image sensor output signals to a fixed voltage, while serial signals are generated by replacing the noise section with the signal section by sample holding the signal section ("B" period) including noises in it. (Refer to Figure 7-3).

- Clamp circuit (CLAMP)
  The noise section ("A" period) of input signal ① is clamped by sample hold 1 (SP1) pulse ② (FCDS, pin ⑫) to a fixed voltage to supply output signal to the sample hold circuit after removing low frequency noises. (Refer to Figure 7-3-(b)-④.)
- Sample hold circuit (SH)
  This is a circuit to sample hold the signal section including noises in it, where the signal section ("B" period) including noises in it is sampled by sample hold 2(SP2) pulse ③ (FS, pin ⑪) and then kept held up to the noise section ("A" period) to generate serial signals by replacing the noise section with the signal section. (Refer to Figure 7-3-(b)-⑤.)
- After being inverted and amplified, the serial signals are supplied to the next gain select circuit.

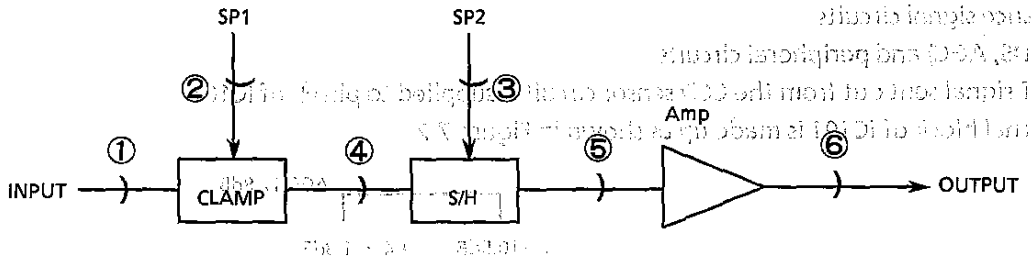


Figure 7-3(a). CDS circuit

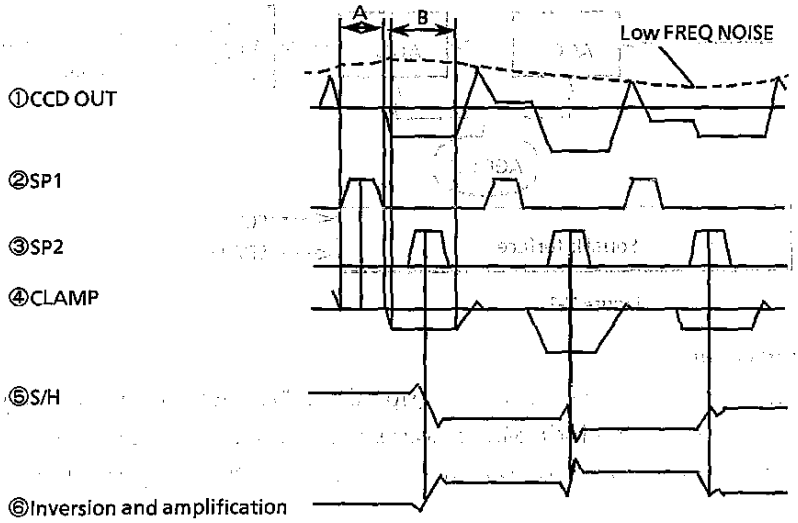


Figure 7-3 (b). CDS time chart

2) AGC gain

By serial transfer of 7-bit data with the microcomputer, AGC gain can be set 0 up to 21dB.

In the internal circuit, 21dB variable width is available in AGC1 (preceding part) and AGC2 (succeeding part). For AGC in this model, AGC2 which is set at the standard +4dB raises GAIN gradually up to +11.3dB, and then AGC1 continues to raise it up to the value from 0dB to 10.5dB. After AGC, it is amplified to +11.7dB before being sent out to pins ⑨ and ⑩.

4) A signal outputted from IC101 is clamped at the set up level (Q103) by PDS CTL DC voltage supplied by XCP1 pulse from pin ④ of D/A converter IC503 before being sent to the subsequent A/D converter IC102.

Also, the adjustment of PDS CTL is made by address 75.

(2) IC102 (A/D converter)

This is 9-bit A/D converter where an analog video signal inputted from pin ㉛ is converted into a digital signal before being sent out to the subsequent IC201 (DSP). (D1 to D9)

SHARP

Printed in Japan